ADC12Jxx00 12-Bit 1.6 or 2.7 GSPS ADCs With Integrated DDC

1 Features

- Excellent Noise and Linearity up to and beyond F_{IN} = 3 GHz
- Configurable DDC
- Decimation Factors from 4 to 32 (Complex Baseband Out)
- Bypass Mode for Full Nyquist Output Bandwidth
- Usable Output Bandwidth of 540 MHz at 4x Decimation and 2700 MSPS
- Usable Output Bandwidth of 320 MHz at 4x Decimation and 1600 MSPS
- Usable Output Bandwidth of 67.5 MHz at 32x Decimation and 2700 MSPS
- Usable Output Bandwidth of 40 MHz at 32x Decimation and 1600 MSPS
- Low Pin-Count JESD204B Subclass 1 Interface
- Automatically Optimized Output Lane Count
- Embedded Low Latency Signal Range Indication
- Low Power Consumption
- **Key Specifications**
  - Max Sampling Rate: 1600 or 2700 MSPS
  - Min Sampling Rate: 1000 MSPS
  - DDC Output Word Size: 15-Bit Complex (30 bits total)
  - Bypass Output Word Size: 12-Bit Offset Binary
  - Noise Floor: –147.3 dBFS/Hz (ADC12J2700)
  - Noise Floor: –145 dBFS/Hz (ADC12J1600)
  - IMD3: −64 dBc (F_{IN} = 2140 MHz ± 30 MHz at −13 dBFS)
  - FPBW (–3 dB): 3.2 GHz
  - Peak NPR: 46 dB
  - Supply Voltages: 1.9 V and 1.2 V
  - Power Consumption
    - Bypass (2700 MSPS): 1.8 W
    - Bypass (1600 MSPS): 1.6 W
    - Power Down Mode: <50 mW

2 Applications

- Wireless Infrastructure
- RF-Sampling Software Defined Radio
- Wideband Microwave Backhaul
- Military Communications
- SIGINT
- RADAR and LIDAR
- DOCSIS / Cable Infrastructure
- Test and Measurement

3 Description

The ADC12J1600 and ADC12J2700 devices are wideband sampling and digital tuning devices. Texas Instruments' giga-sample analog-to-digital converter (ADC) technology enables a large block of frequency spectrum to be sampled directly at RF. An integrated DDC (Digital Down Converter) provides digital filtering and down-conversion. The selected frequency block is made available on a JESD204B serial interface. Data is output as baseband 15-bit complex information for ease of downstream processing. Based on the digital down-converter (DDC) decimation and link output rate settings, this data is output on 1 to 5 lanes of the serial interface.

A DDC bypass mode allows the full rate 12-bit raw ADC data to also be output. This mode of operation requires 8 lanes of serial output.

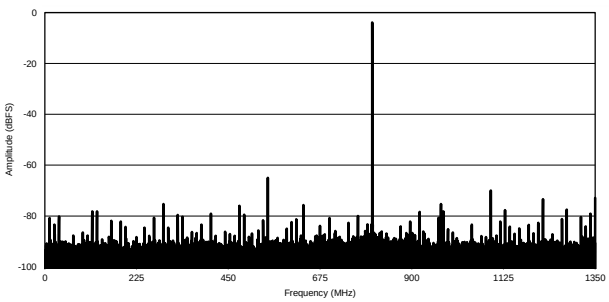
The ADC12J1600 and ADC12J2700 devices are available in a 68-pin VQFN package. The device operates over the Industrial (–40°C ≤ T_A ≤ 85°C) ambient temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC12J1600	VQFN (68)	10.00 mm × 10.00 mm
ADC12J2700	VQFN (68)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Bypass — Spectral Response
f_S = 2.7 GHz, F_{IN} = 1897 MHz at –1 dBFS



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision B (September 2014) to Revision C — **Page**

- Added additional voltage difference parameters to the *Absolute Maximum Ratings* table ... 8
- Added junction temperature to the *Absolute Maximum Ratings* table ... 8
- Added common mode voltage parameter to the *Recommended Operating Conditions* table. Changed CLK to SYSREF, and ~SYNC ... 9
- Changed some of the maximum interleaving offset values for both devices to tighten the levels ... 10
- Deleted the *Differential Analog Input Connection* image in *The Analog Inputs* section ... 31
- Added note about offset adjust in Background Calibration Mode to the *Offset Adjust* section and I/O offset register tables ... 35
- Added the *Calibration Cycle Timing for Different Calibration Modes and Options* table in the *Timing Calibration Mode* section ... 50
- Changed 0x004-0x005 to RESERVED in the *Standard SPI-3.0 Registers* summary table ... 60

Changes from Revision A (February 2014) to Revision B — **Page**

- Changed the device status from *Product Preview* to *Production Data* ... 1

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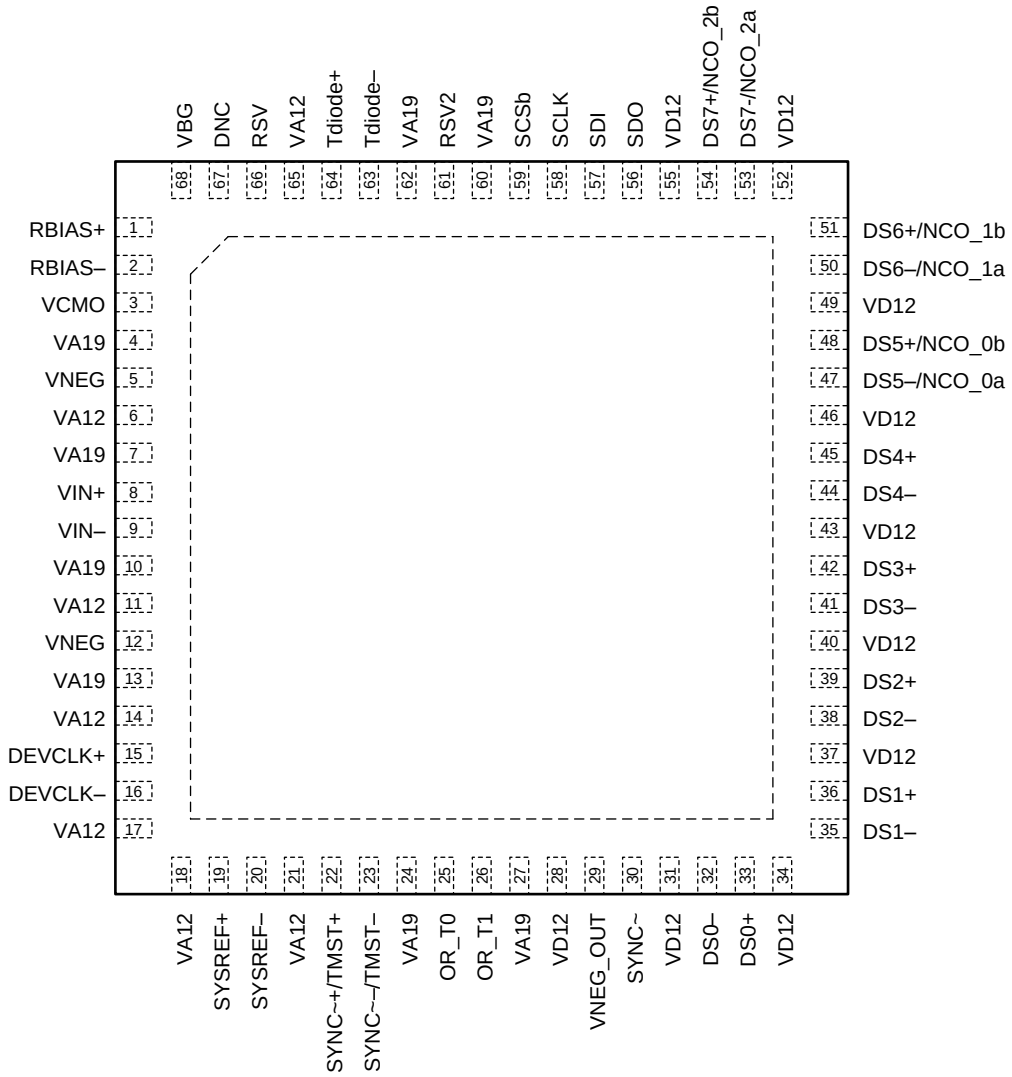
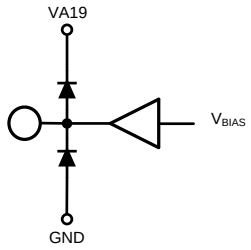
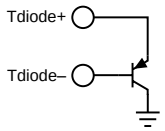
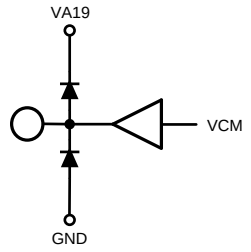
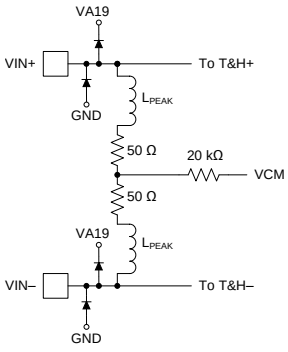
5 Pin Configuration and Functions

NKE Package
68-Pin VQFN With Thermal Pad
Top View



DNC = Make no external connection

Pin Functions

PIN		EQUIVALENT CIRCUIT	TYPE	DESCRIPTION
NAME	NO.			
ANALOG				
RBIAS+	1		I/O	**External Bias Resistor Connections** External bias resistor terminals. A 3.3 kΩ (±0.1%) resistor should be connected between RBIAS+ and RBIAS–. The RBIAS resistor is used as a reference for internal circuits which affect the linearity of the converter. The value and precision of this resistor should not be compromised. These pins must be isolated from all other signals and grounds.
RBIAS–	2			
TDIODE–	63		Passive	**Temperature Diode** These pins are the positive (anode) and negative (cathode) diode connections for die temperature measurements. Leave these pins unconnected if they are not used. See the *Built-In Temperature Monitor Diode* section for more details.
TDIODE+	64			
VBG	68		O	**Bandgap Output Voltage** This pin is capable of sourcing or sinking 100 µA and can drive a load up to 80 pF. Leave this pin unconnected if it is not used in the application. See the *The Reference Voltage* section for more details.
VCMO	3		O	**Common Mode Voltage** The voltage output at this pin must be the common-mode input voltage at the VIN+ and VIN– pins when DC coupling is used. This pin is capable of sourcing or sinking 100 µA and can drive a load up to 80 pF. Leave this pin unconnected if it is not used in the application.
VIN+	8		I	**Signal Input** The differential full-scale input range is determined by the full-scale voltage adjust register. An internal peaking inductor (L_{PEAK}) of 5 nH is included for parasitic compensation.
VIN–	9			

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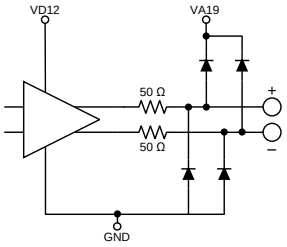
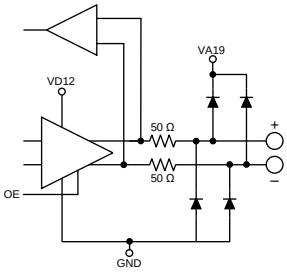
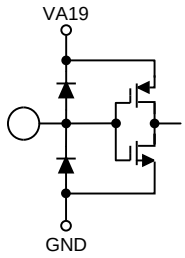
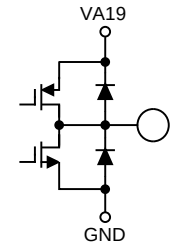
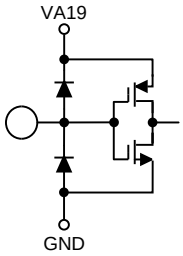
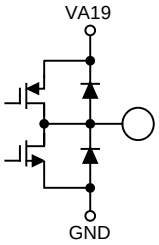
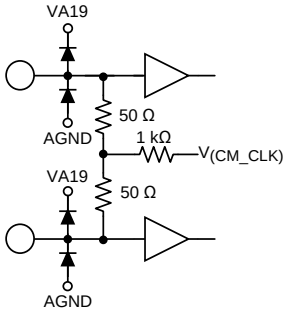
Pin Functions (continued)

PIN		EQUIVALENT CIRCUIT	TYPE	DESCRIPTION
NAME	NO.			
DATA				
DS0–	32		O	**Data** **CML** These pins are the high-speed serialized-data outputs with user-configurable pre-emphasis. These outputs must always be terminated with a 100-Ω differential resistor at the receiver.
DS0+	33			
DS1–	35			
DS1+	36			
DS2–	38			
DS2+	39			
DS3–	41			
DS3+	42			
DS4–	44			
DS4+	45			
DS5–/NCO_0	47		O/I	**Data** **DS5–/NCO_0, DS5+/NCO_0, DS6–/NCO_1, DS6+/NCO_1, DS7–/NCO_2 and DS7+/NCO_2**: When decimation is enabled, these pins become LVCMOS inputs and allow the host device to select the specific NCO frequency or phase accumulator that is active. In this mode the positive (+) and negative (–) pins should be connected together and both driven. An acceptable alternative is to let one of the pair float while the other pin is driven. Connect these inputs to GND if they are not used in the application.
DS5+/NCO_0	48			
DS6−/NCO_1	50			
DS6+/NCO_1	51			
DS7−/NCO_2	53			
DS7+/NCO_2	54			
GROUND, RESERVED, DNC				
DNC	67		—	**Do Not Connect** Do not connect DNC to any circuitry, power, or ground signals.
RSV	66		—	**Reserved** **Connect to Ground or Leave Unconnected:** This reserved pin is a logic input for possible future device versions. It is recommended to connect this pin to ground. Floating this pin is also permissible.
RSV2	61		—	**Reserved** **Connect to Ground** Connect this reserved input pin to ground for proper operation.
Thermal Pad			—	**Ground (GND)** The exposed pad on the bottom of the package is the ground return for all supplies. This pad must be connected with multiple vias to the printed circuit board (PCB) ground planes to ensure proper electrical and thermal performance. The exposed center pad on the bottom of the package must be thermally and electrically connected (soldered) to a ground plane to ensure rated performance.
LVCMOS				
OR_T0	25		O	**Over-Range** Over-range detection status for T0 and T1 thresholds. Leave these pins unconnected if they are not used in the application.
OR_T1	26			

Pin Functions (continued)

PIN		EQUIVALENT CIRCUIT	TYPE	DESCRIPTION
NAME	NO.			
SCLK	58		I	**Serial Interface Clock** This pin functions as the serial-interface clock input which clocks the serial data in and out. The *Using the Serial Interface* section describes the serial interface in more detail.
SDI	57		I	**Serial Data In** This pin functions as the serial-interface data input. The *Using the Serial Interface* section describes the serial interface in more detail.
SYNC~	30		I	**SYNC~** This pin provides the JESD204B-required synchronizing request input. A logic-low applied to this input initiates a lane alignment sequence. The choice of LVCMOS or differential SYNC~ is selected through bit 6 of the configuration register 0x202h. Connect this input to GND or VA19 if differential SYNC~ input is used.
$\overline{\text{SCS}}$	59		I	**Serial Chip Select (active low)** This pin functions as the serial-interface chip select. The *Using the Serial Interface* section describes the serial interface in more detail.
SDO	56		O	**Serial Data Out** This pin functions as the serial-interface data output. The *Using the Serial Interface* section describes the serial interface in more detail.
DIFFERENTIAL INPUT				
DEVCLK+	15		I	**Device Clock Input** The differential device clock signal must be AC coupled to these pins. The input signal is sampled on the rising edge of CLK.
DEVCLK–	16			
SYSREF+	19		I	**SYSREF** The differential periodic waveform on these pins synchronizes the device per JESD204B. If JESD204B subclass 1 synchronization is not required and these inputs are not utilized they may be left unconnected. In that case ensure SysRef_Rcvr_En=0 and SysRef_Pr_En=0.
SYSREF–	20			
SYNC~+/TMST+	22		I	**SYNC~/TMST** This differential input provides the JESD204B-required synchronizing request input. A differential logic-low applied to these inputs initiates a lane alignment sequence. For differential SYNC~ usage, ensure that SYNC_DIFF_PD = 0 and SYNC_DIFFSEL = 1. When the LVCMOS SYNC~ is selected these inputs can be used as the differential TIMESTAMP input. For TMST usage, ensure that SYNC_DIFF_PD = 0, SYNC_DIFFSEL = 0, and TIME_STAMP_EN = 1. For additional information see the *Time Stamp* section. These inputs may be left unconnected if they are not used for either the SYNC~ or TIMESTAMP functions.
SYNC~-/TMST–	23			

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Pin Functions (continued)

PIN		EQUIVALENT CIRCUIT	TYPE	DESCRIPTION
NAME	NO.			
POWER				
VA12	6 11 14 17 18 21 65		—	**Analog 1.2 V power supply pins** Bypass these pins to ground using one 10-µF capacitor and two 1-µF capacitors for bulk decoupling plus one 0.1-µF capacitor per pin for individual decoupling.
VA19	4 7 10 13 24 27 60 62		—	**Analog 1.9 V power supply pins** Bypass these pins to ground using one 10-µF capacitor and two 1-µF capacitors for bulk decoupling plus one 0.1-µF capacitor per pin for individual decoupling.
VD12	28 31 34 37 40 43 46 49 52 55		—	**Digital 1.2 V power supply pins** Bypass these pins to ground using one 10-µF capacitor and two 1-µF capacitors for bulk decoupling plus one 0.1-µF capacitor per pin for individual decoupling.
VNEG	5 12		I	**VNEG** These pins must be decoupled to ground with a 0.1-µF ceramic capacitor near each pin. These power input pins must be connected to the VNEG_OUT pin with a low resistance path. The connections must be isolated from any noisy digital signals and must also be isolated from the analog input and clock input pins.
VNEG_OUT	29		O	**VNEG_OUT** The voltage on this output can range from –1V to +1V. This pin must be decoupled to ground with a 4.7-µF, low ESL, low ESR multi-layer ceramic chip capacitor and connected to the VNEG input pins. This voltage must be isolated from any noisy digital signals, clocks, and the analog input.

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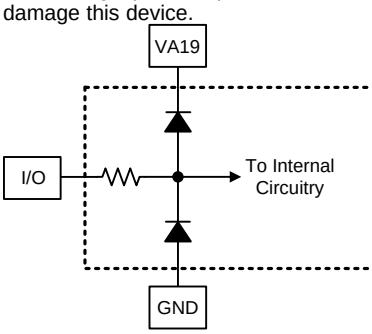
6 Specifications

6.1 Absolute Maximum Ratings

The soldering process must comply with TI's Reflow Temperature Profile specifications. Refer to www.ti.com/packaging. (1) (2) (3)

			MIN	MAX	UNIT
Supply voltage	1.2-V supply	VA12, VD12		1.4	V
	1.9-V supply	VA19		2.2	V
	1.2-V supply difference between VA12 and VD12		–200	200	mV
Voltage	On any input pin (except VIN+ or VIN–)		–0.15	$V_{(VA19)}$ + 0.15	V
	On VIN+ or VIN–		0	2	V
Voltage difference	|(VIN+) – (VIN–)| (4)			2	V
	|(DEVCLK+) – (DEVCLK–)|			2	
	|(SYSREF+) – (SYSREF–)|			2	
	|(~SYNC+) – (~SYNC–)|			1	
RF input power, P_I	On VIN+, VIN–, with proper input common mode maintained. F_{IN} ≥ 3 GHz, $Z_{(SOURCE)}$ = 100 Ω, Input_Clamp_EN = 0 or 1			11.07	dBm
	On VIN+, VIN–, with proper input common mode maintained. F_{IN} = 1 GHz, $Z_{(SOURCE)}$ = 100 Ω, Input_Clamp_EN = 1			14.95	
	On VIN+, VIN–, with proper input common mode maintained. F_{IN} ≤ 100 MHz, $Z_{(SOURCE)}$ = 100 Ω, Input_Clamp_EN = 1			20.97	
Input current	At any pin other than VIN+ or VIN– (5)		–25	25	mA
	VIN+ or VIN–		–50	50	mA DC
	Package (5) (sum of absolute value of all currents forced in or out, not including power supply current)			100	mA
Junction temperature, T_J	Power applied. Verified by High Temperature Operation Life testing to 1000 hours.		–40	150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Reflow temperature profiles are different for lead-free and non-lead-free packages.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The analog inputs are protected as in the following circuit. Input-voltage magnitudes beyond the *Absolute Maximum Ratings* may damage this device.



(5) When the input voltage at any pin (other than VIN+ or VIN–) exceeds the power supply limits (that is, less than GND or greater than VA19), the current at that pin must be limited to 25 mA. The 100-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies. This limit is not placed upon the power pins or thermal pad (GND).

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

All voltages are measured with respect to GND = 0 V, unless otherwise specified.

			MIN	MAX	UNIT
V_{DD}	Supply voltage	1.2-V supply: VA12, VD12	1.14	1.26	V
		1.9-V supply: VA19	1.8	2	V
	Supply sequence (power-up and power-down)			1.9 supply ≥ 1.2 supply	V
V_{CMI}	Analog input common mode voltage		$V_{(VCMO)}$ – 0.15	$V_{(VCMO)}$ + 0.15	V
	VIN+, VIN– voltage (maintaining common mode)		0	$V_{(VA19)}$	V
	DEVCLK±, SYSREF±, ~SYNC± pin voltage range		0	$V_{(VA19)}$	V
$V_{ID(CLK)}$	Differential DEVCLK±, SYSREF±, ~SYNC± amplitude		0.4	2	V_{PP}
$V_{CM(CLK)}$	SYSREF±, ~SYNC± Common Mode		0.64	1.1	V
T_A	Ambient temperature		–40	85	°C
T_J	Junction temperature			135	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADC12J1x00 NKE (VQFN) 68 PINS	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	19.8	°C/W
$R_{\theta JCbot}$	Thermal resistance, junction-to-case (bottom)	2.7	°C/W
ψ_{JB}	Characterization parameter, junction-to-board	9.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 mV_{PP}), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at T_A = 25°C.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE CHARACTERISTICS						
RES	ADC core resolution	Resolution with no missing codes		12		bits
INL	Integral non-linearity	T_A = 25°C		±2		LSB
		T_A = T_{MIN} to T_{MAX}		±3		
DNL	Differential non-linearity	T_A = 25°C		±0.25		LSB
		T_A = T_{MIN} to T_{MAX}		±0.3		
Peak NPR	Peak noise power ratio	500-kHz tone spacing from 1 MHz to f_S / 2−1 MHz, DDC bypass mode 25-MHz wide notch at 320 MHz		46		dB
IMD_3	Third-order intermodulation distortion	F1 = 2110 MHz at −13 dBFS F2 = 2170 MHz at −13 dBFS		–64		dBc

(1) To ensure accuracy, the VA19, VA12, and VD12 pins are required to be well bypassed. Each supply pin must be decoupled with one or more bypass capacitors.
(2) Interleave related fixed frequency spurs at f_S / 4 and f_S / 2 are excluded from all SNR, SINAD, ENOB and SFDR specifications. The magnitude of these spurs is provided separately.

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Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 mV_{PP}), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at T_A = 25°C.[1][2]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DDC BYPASS Mode, ADC12J2700, $f_{(DEVCLK)}$ = 2.7 GHz							
SNR	Signal-to-noise ratio, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			55.1		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		54.9		
			T_A = T_{MIN} to T_{MAX}	52.5			
			T_A = 25°C, calibration = BG		54.8		
			T_A = T_{MIN} to T_{MAX}, calibration = BG	52.4			
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			52.5		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			50		
SINAD	Signal-to-noise and distortion ratio, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			55		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		54.8		
			T_A = T_{MIN} to T_{MAX}	52.3			
			T_A = 25°C, calibration = BG		54.7		
			T_A = T_{MIN} to T_{MAX}, calibration = BG	52.2			
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			52.4		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			50		
ENOB	Effective number of bits, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			8.8		Bits
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		8.8		
			T_A = T_{MIN} to T_{MAX}	8.4			
			T_A = 25°C, calibration = BG		8.8		
			T_A = T_{MIN} to T_{MAX}, calibration = BG	8.4			
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			8.4		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			8		
SFDR	Spurious-free dynamic range Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			66.7		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		71.6		
			T_A = T_{MIN} to T_{MAX}	61			
			T_A = 25°C, calibration = BG		70		
			T_A = T_{MIN} to T_{MAX}, calibration = BG	59			
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			65.2		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			58.6		
$f_S/2$	Interleaving offset spur at ½ sampling rate	F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–77		dBFS
			T_A = T_{MIN} to T_{MAX}			–59.5	
			T_A = 25°C, calibration = BG		–74		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–57.5	
$f_S/4$	Interleaving offset spur at ¼ sampling rate	F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–70		dBFS
			T_A = T_{MIN} to T_{MAX}			–54.5	
			T_A = 25°C, calibration = BG		–68		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–53	
$f_S/2 – F_{IN}$	Interleaving offset spur at ½ sampling rate – input frequency	F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–78		dBFS
			T_A = T_{MIN} to T_{MAX}			–62	
			T_A = 25°C, calibration = BG		–76		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–61	
$f_S/4 + F_{IN}$	Interleaving offset spur at ¼ sampling rate + input frequency	F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–76		dBFS
			T_A = T_{MIN} to T_{MAX}			–61	
			T_A = 25°C, calibration = BG		–71		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–59	
$f_S/4 – F_{IN}$	Interleaving offset spur at ¼ sampling rate – input frequency	F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–77		dBFS
			T_A = T_{MIN} to T_{MAX}			–61.4	
			T_A = 25°C, calibration = BG		–76		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–61	

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Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 mV_{PP}), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at T_A = 25°C.(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			–73		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–70		
			T_A = T_{MIN} to T_{MAX}			–61	
			T_A = 25°C, calibration = BG		–72		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–62	
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			–68		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			–68		
HD2	Second harmonic distortion	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			–72		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–79		
			T_A = T_{MIN} to T_{MAX}			–62	
			T_A = 25°C, calibration = BG		–81		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–64	
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			–76		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			–70		
HD3	Third harmonic distortion	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			–72		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–75		
			T_A = T_{MIN} to T_{MAX}			–63	
			T_A = 25°C, calibration = BG		–81		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–64	
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			–70		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			–76		
NSD	Noise spectral density, average NSD across Nyquist bandwidth	12-bit DDC bypass mode, ADC12J2700, $f_{(DEVCLK)}$ = 2.7 GHz	50-Ω AC-coupled terminated input		–147.3		dBFS/Hz
					–149.1		dBm/Hz
			F_{IN} = 600 MHz, –1 dBFS		–146.2		dBFS/Hz
					–148.0		dBm/Hz
DDC BYPASS MODE, ADC12J1600, $f_{(DEVCLK)}$ = 1.6 GHz							
SNR	Signal-to-noise ratio, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			55.3		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		54.9		
			T_A = T_{MIN} to T_{MAX}	52.3			
			T_A = 25°C, calibration = BG		54.8		
			T_A = T_{MIN} to T_{MAX}, calibration = BG	52.2			
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			52.5		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			49.8		
SINAD	Signal-to-noise and distortion ratio, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			55.2		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		54.8		
			T_A = T_{MIN} to T_{MAX}	52.1			
			T_A = 25°C, calibration = BG		54.7		
			T_A = T_{MIN} to T_{MAX}, calibration = BG	52			
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			52.4		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			49.7		
ENOB	Effective number of bits, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			8.9		Bits
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		8.8		
			T_A = T_{MIN} to T_{MAX}	8.4			
			T_A = 25°C, calibration = BG		8.8		
			T_A = T_{MIN} to T_{MAX}, calibration = BG	8.4			
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			8.4		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			8		

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Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 mV_{PP}), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at T_A = 25°C.[1][2]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SFDR	Spurious-free dynamic range Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			72.9		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		74.8		
			T_A = T_{MIN} to T_{MAX}			61.8	
			T_A = 25°C, calibration = BG		71		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			60.7	
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			66.7		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			59.8		
$f_S/2$	Interleaving offset spur at ½ sampling rate	F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–77		dBFS
			T_A = T_{MIN} to T_{MAX}			–59.8	
			T_A = 25°C, calibration = BG		–73		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–57.3	
$f_S/4$	Interleaving offset spur at ¼ sampling rate	F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–72		dBFS
			T_A = T_{MIN} to T_{MAX}			–54.3	
			T_A = 25°C, calibration = BG		–69		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–54	
$f_S/2 – F_{IN}$	Interleaving offset spur at ½ sampling rate – input frequency	F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–77		dBFS
			T_A = T_{MIN} to T_{MAX}			–62	
			T_A = 25°C, calibration = BG		–79		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–62	
$f_S/4 + F_{IN}$	Interleaving offset spur at ¼ sampling rate + input frequency	F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–76		dBFS
			T_A = T_{MIN} to T_{MAX}			–61.8	
			T_A = 25°C, calibration = BG		–74		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–61	
$f_S/4 – F_{IN}$	Interleaving offset spur at ¼ sampling rate – input frequency	F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–76		dBFS
			T_A = T_{MIN} to T_{MAX}			–62	
			T_A = 25°C, calibration = BG		–77		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–61	
THD	Total harmonic distortion	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			–72		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–72		
			T_A = T_{MIN} to T_{MAX}			–60.9	
			T_A = 25°C, calibration = BG		–71		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–61	
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			–69		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			–69		
HD2	Second harmonic distortion	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			–79		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–78		
			T_A = T_{MIN} to T_{MAX}			–62	
			T_A = 25°C, calibration = BG		–79		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–63	
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			–73		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			–70		
HD3	Third harmonic distortion	F_{IN} = 350 MHz, –1 dBFS, 12-bit DDC bypass mode			–76		dBFS
		F_{IN} = 600 MHz, –1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		–81		
			T_A = T_{MIN} to T_{MAX}			–65	
			T_A = 25°C, calibration = BG		–76		
			T_A = T_{MIN} to T_{MAX}, calibration = BG			–61	
		F_{IN} = 1500 MHz, –1 dBFS, 12-bit DDC bypass mode			–72		
		F_{IN} = 2400 MHz, –1 dBFS, 12-bit DDC bypass mode			–76		

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Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 mV_{PP}), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at T_A = 25°C.(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NSD	Noise spectral density, average NSD across Nyquist bandwidth	12-bit DDC bypass mode, ADC12J1600, $f_{(DEVCLK)}$ = 1.6 GHz	50-Ω AC-coupled terminated input		–145		dBFS/Hz
					–146.8		dBm/Hz
			F_{IN} = 600 MHz, –1 dBFS		–143.9		dBFS/Hz
					–145.7		dBm/Hz
DECIMATE-BY-8 MODE, ADC12J2700, $f_{(DEVCLK)}$ = 2.7 GHz							
SNR	Signal-to-noise ratio, integrated across DDC output bandwidth Interleaving spurs included	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			62.8		dBFS
			Calibration = BG		62.7		
		F_{IN} = 2400 MHz, –1 dBFS, Decimate-by-8 mode			53.3		
SINAD	Signal-to-noise and distortion ratio, integrated across DDC output bandwidth Interleaving spurs included	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			62.8		dBFS
			Calibration = BG		62.7		
		F_{IN} = 2400 MHz, –1 dBFS, decimate-by-8 mode			53.3		
ENOB	Effective number of bits, integrated across DDC output bandwidth Interleaving spurs included	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			10.1		Bits
			Calibration = BG		10.1		
		F_{IN} = 2400 MHz, –1 dBFS, decimate-by-8 mode			8.6		
SFDR	Spurious-free dynamic range Interleaving spurs included	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			75.9		dBFS
			Calibration = BG		74.7		
$f_S/2$	Interleaving offset spur at ½ sampling rate(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–73		dBFS
			Calibration = BG		–72		
$f_S/4$	Interleaving offset spur at ¼ sampling rate(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–70		dBFS
			Calibration = BG		–70		
$f_S/2 – F_{IN}$	Interleaving spur at ½ sampling rate – input frequency(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–80		dBFS
			Calibration = BG		–79		
$f_S/4 + F_{IN}$	Interleaving spur at ¼ sampling rate + input frequency(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–73		dBFS
			Calibration = BG		–70		
$f_S/4 – F_{IN}$	Interleaving spur at ¼ sampling rate – input frequency(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–77		dBFS
			Calibration = BG		–77		
THD	Total harmonic distortion(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–70		dBFS
			calibration = BG		–71		
		F_{IN} = 2400 MHz, –1 dBFS, decimate-by-8 mode			–65		
HD2	Second harmonic distortion(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–78		dBFS
			Calibration = BG		–76		
		F_{IN} = 2400 MHz, –1 dBFS, decimate-by-8 mode			–67		
HD3	Third harmonic distortion(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–74		dBFS
			Calibration = BG		–81		
		F_{IN} = 2400 MHz, –1 dBFS, decimate-by-8 mode			–73		
DECIMATE-BY-8 MODE, ADC12J1600, $f_{(DEVCLK)}$ = 1.6 GHz							
SNR	Signal-to-noise ratio, integrated across DDC output bandwidth Interleaving spurs included	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			63.5		dBFS
			Calibration = BG		63.4		
		F_{IN} = 2400 MHz, –1 dBFS, decimate-by-8 mode			55.8		
SINAD	Signal-to-noise and distortion ratio, integrated across DDC output bandwidth Interleaving spurs included	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			63.5		dBFS
			Calibration = BG		63.4		
		F_{IN} = 2400 MHz, –1 dBFS, decimate-by-8 mode			55.8		
ENOB	Effective number of bits, integrated across DDC output bandwidth Interleaving spurs included	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			10.3		Bits
			Calibration = BG		10.2		
		F_{IN} = 2400 MHz, –1 dBFS, decimate-by-8 mode			9.0		
SFDR	Spurious-free dynamic range Interleaving Spurs Included	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			76.2		dBFS
			Calibration = BG		76.7		
$f_S/2$	Interleaving offset spur at ½ sampling rate(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–73		dBFS
			Calibration = BG		–72		

(3) Magnitude of reported tones in output spectrum of ADC core. This tone will only be present in the DDC output for specific Decimation and NCO settings. Careful frequency planning can be used to intentionally place unwanted tones outside the DDC output spectrum.

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Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 mV_{PP}), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at T_A = 25°C.(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_S/4$	Interleaving offset spur at ¼ sampling rate(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–70		dBFS
			Calibration = BG		–69		
$f_S/2 – F_{IN}$	Interleaving spur at ½ sampling rate – input frequency(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–78		dBFS
			Calibration = BG		–79		
$f_S/4 + F_{IN}$	Interleaving spur at ¼ sampling rate + input frequency(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–76		dBFS
			Calibration = BG		–77		
$f_S/4 – F_{IN}$	Interleaving spur at ¼ sampling rate – input frequency(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–77		dBFS
			Calibration = BG		–72		
THD	Total harmonic distortion(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–71		dBFS
			Calibration = BG		–71		
		F_{IN} = 2400 MHz, –1 dBFS, decimate-by-8 mode			–63		
HD2	Second harmonic distortion(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–77		dBFS
			Calibration = BG		–78		
		F_{IN} = 2400 MHz, –1 dBFS, decimate-by-8 mode			–65		
HD3	Third harmonic distortion(3)	F_{IN} = 600 MHz, –1 dBFS, decimate-by-8 mode			–80		dBFS
			Calibration = BG		–77		
		F_{IN} = 2400 MHz, –1 dBFS, decimate-by-8 mode			–74		
DDC CHARACTERISTICS							
	Alias protection(4)			80			dB
	Alias protected bandwidth(4)			80			% of output BW
SFDR-DDC	Spurious-free dynamic range of digital down-converter(4)			100			dB
	Implementation loss(4)					0.5	dB
ANALOG INPUT CHARACTERISTICS							
$V_{ID(VIN)}$	Full-scale analog-differential input range	Minimum FSR setting(5)			500		mV_{PP}
		Default FSR setting, T_A = T_{MIN} to T_{MAX}		650	725	800	
		Maximum FSR setting(5)			950		
$C_{I(VIN)}$	Analog input capacitance(4)	Differential			0.05		pF
		Each input pin to ground			1.5		pF
$R_{ID(VIN)}$	Differential input resistance			80	95	110	Ω
FPBW	Full power bandwidth	–3 dB — calibration = BG			2.8		GHz
		–3 dB — calibration = FG			3.2		
	Gain flatness	DC to 2 GHz			1.2		dB
		2 GHz to 4 GHz			3.8		
		DC to 2 GHz — calibration = BG			1.5		
		2 GHz to 4 GHz — calibration = BG			4.5		
ANALOG OUTPUT CHARACTERISTICS (VCMO, VBG)							
$V_{(VCMO)}$	Common-mode output voltage	$I_{(VCMO)}$ = ±100 µA, T_A = 25°C			1.225		V
		$I_{(VCMO)}$ = ±100 µA, T_A = T_{MIN} to T_{MAX}		1.185		1.265	
$TCV_{O(VCMO)}$	Common-mode output-voltage temperature coefficient	T_A = T_{MIN} to T_{MAX}			-21		ppm/°C
$C_{(LOAD\_VCMO)}$	Maximum VCMO output load capacitance					80	pF
$V_{O(BG)}$	Bandgap reference output voltage	$I_{(BG)}$ = ±100 µA, T_A = 25°C			1.248		V
		$I_{(BG)}$ = ±100 µA, T_A = T_{MIN} to T_{MAX}		1.195		1.3	
$TCV_{ref(BG)}$	Bandgap reference voltage temperature coefficient	T_A = T_{MIN} to T_{MAX}, $I_{(BG)}$ = ±100 µA			0		ppm/°C
$C_{(LOAD\_BG)}$	Maximum bandgap reference output load capacitance					80	pF

(4) This parameter is specified by design and is not tested in production.
(5) This parameter is specified by design, characterization, or both and is not tested in production.

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Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 mV_{PP}), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at T_A = 25°C.(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TEMPERATURE DIODE CHARACTERISTICS							
$V_{(TDIODE)}$	Temperature diode voltage slope	Offset voltage (approx. 0.77 V) varies with process and must be measured for each part. Offset measurement should be done with PowerDown=1 to minimize device self-heating.	100-µA forward current Device active		–1.6		mV/°C
			100-µA forward current Device in power-down		–1.6		mV/°C
CLOCK INPUT CHARACTERISTICS (DEVCLK±, SYSREF±, SYNC~/TMST±)							
$V_{ID(CLK)}$	Differential clock input level	Sine wave clock, T_A = T_{MIN} to T_{MAX}		0.4	0.6	2	V_{PP}
		Square wave clock, T_A = T_{MIN} to T_{MAX}		0.4	0.6	2	V_{PP}
$I_{I(CLK)}$	Input current	V_I = 0 or V_I = V_A			±1		µA
$C_{I(CLK)}$	Input capacitance(4)	Differential			0.02		pF
		Each input to ground			1		pF
$R_{ID(CLK)}$	Differential input resistance	T_A = 25°C			95		Ω
		T_A = T_{MIN} to T_{MAX}		80		110	Ω
CML OUTPUT CHARACTERISTICS (DS0–DS7±)							
V_{OD}	Differential output voltage	Assumes ideal 100-Ω load Measured differentially Default pre-emphasis setting		280	305	330	mV peak
$V_{O(ofs)}$	Output offset voltage				0.6		V
I_{OS}	Output short-circuit current	Output+ and output– shorted together			±6		mA
		Output+ or output– shorted to 0 V			12		
Z_{OD}	Differential output impedance				100		Ω
LVCMOS INPUT CHARACTERISTICS (SDI, SCLK, $\overline{SCS}$, SYNC~)							
V_{IH}	Logic high input voltage	See (5)		0.83			V
V_{IL}	Logic low input voltage	See (5)				0.4	V
C_I	Input capacitance(4)(6)	Each input to ground			1		pF
LVCMOS OUTPUT CHARACTERISTICS (SDO, OR_T0, OR_T1)							
V_{OH}	CMOS H level output	I_{OH} = –400 µA(5)		1.65	1.9		V
V_{OL}	CMOS L level output	I_{OH} = 400 µA(5)			0.01	0.15	V
POWER SUPPLY CHARACTERISTICS							
ADC12J2700, $f_{(DEVCLK)}$ = 2.7 GHz							
$I_{(VA19)}$	Analog 1.9-V supply current	PD = 0, calibration = FG, bypass DDC			457	495	mA
		PD = 0, calibration = BG, bypass DDC			557	594	
		PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1			557	598	
$I_{(VA12)}$	Analog 1.2-V supply current	PD = 0, calibration = FG, bypass DDC			245	296	mA
		PD = 0, calibration = BG, bypass DDC			261	312	
		PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1			270	322	
$I_{(VD12)}$	Digital 1.2-V supply current	PD = 0, calibration = FG, bypass DDC			330	541	mA
		PD = 0, calibration = BG, bypass DDC			341	588	
		PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1			366	610	
P_C	Power consumption	PD = 0, calibration = FG, bypass DDC			1.56	1.94	W
		PD = 0, calibration = BG, bypass DDC			1.78	2.21	
		PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1			1.82	2.25	
		PD = 1			< 50		mW

(6) The digital control pin capacitances are die capacitances only and is in addition to package and bond-wire capacitance of approximately 0.4 pF.

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Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 mV_{PP}), VIN = –1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at T_A = 25°C.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC12J1600, $f_{(DEVCLK)}$ = 1.6 GHz						
$I_{(VA19)}$	Analog 1.9-V supply current	PD = 0, calibration = FG, bypass DDC		454	493	mA
		PD = 0, calibration = BG, bypass DDC		553	591	
		PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1		553	598	
$I_{(VA12)}$	Analog 1.2-V supply current	PD = 0, calibration = FG, bypass DDC		180	222	mA
		PD = 0, calibration = BG, bypass DDC		190	233	
		PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1		196	243	
$I_{(VD12)}$	Digital 1.2-V supply current	PD = 0, calibration = FG, bypass DDC		225	460	mA
		PD = 0, calibration = BG, bypass DDC		237	529	
		PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1		255	568	
P_C	Power consumption	PD = 0, calibration = FG, bypass DDC		1.35	1.75	W
		PD = 0, calibration = BG, bypass DDC		1.56	2.04	
		PD = 0, calibration = BG, decimate by 8, DDR = 0, P54 = 1		1.59	2.11	
		PD = 1		< 50		mW

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
DEVICE (SAMPLING) CLOCK						
$f_{(DEVCLK)}$	Input DEVCLK frequency	Sampling rate is equal to clock input, ADC12J2700	1		2.7	GHz
		Sampling rate is equal to clock input, ADC12J1600	1		1.6	
$t_{d(A)}$	Sampling (aperture) delay	Input CLK transition to sampling instant		0.64		ns
$t_{(AJ)}$	Aperture jitter			0.1		ps RMS
$t_{(LAT)}$	ADC core latency(1)	Decimation = 1, DDR = 1, P54 = 0		64		$t_{(DEVCLK)}$
$t_{(LAT\_DDC)}$	ADC core and DDC latency(1)	Decimation = 4, DDR = 1, P54 = 0		292		$t_{(DEVCLK)}$
		Decimation = 4, DDR = 1, P54 = 1		284		
		Decimation = 8, DDR = 0, P54 = 0		384		
		Decimation = 8, DDR = 0, P54 = 1		368		
		Decimation = 8, DDR = 1, P54 = 0		392		
		Decimation = 8, DDR = 1, P54 = 1		368		
		Decimation = 10, DDR = 0, P54 = 0		386		
		Decimation = 10, DDR = 1, P54 = 0		386		
		Decimation = 16, DDR = 0, P54 = 0		608		
		Decimation = 16, DDR = 0, P54 = 1		560		
		Decimation = 16, DDR = 1, P54 = 0		608		
		Decimation = 16, DDR = 1, P54 = 1		560		
		Decimation = 20, DDR = 0, P54 = 0		568		
		Decimation = 20, DDR = 1, P54 = 0		568		
		Decimation = 32, DDR = 0, P54 = 0		1044		
		Decimation = 32, DDR = 0, P54 = 1		948		
		Decimation = 32, DDR = 1, P54 = 0		1044		

(1) Unless otherwise specified, delays quoted are exact un-rounded functional delays (assuming zero propagation delay).

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Timing Requirements (continued)

			MIN	NOM	MAX	UNIT
JESD204B INTERFACE LINK TIMING CHARACTERISTICS (REFER TO Figure 1)						
$t_{d(LMFC)}$	SYSREF to LMFC delay Functional delay between SYSREF assertion latched and LMFC frame boundary(1)	All decimation modes		40		$t_{(DEVCLK)}$
$t_{d(TX)}$	LMFC to frame boundary delay - DDC bypass mode Functional delay from LMFC frame boundary to beginning of next multi-frame in transmitted data.(2)	Decimation = 1, DDR = 1, P54 = 0		52.7		$t_{(DEVCLK)}$
$t_{d(TX)}$	LMFC to frame boundary delay - decimation modes Functional delay from LMFC frame boundary to beginning of next multi-frame in transmitted data(2)	Decimation = 4, DDR = 1, P54 = 0		52.7		$t_{(DEVCLK)}$
		Decimation = 4, DDR = 1, P54 = 1		43.9		
		Decimation = 8, DDR = 0, P54 = 0		60.7		
		Decimation = 8, DDR = 0, P54 = 1		51.5		
		Decimation = 8, DDR = 1, P54 = 0		52.7		
		Decimation = 8, DDR = 1, P54 = 1		43.9		
		Decimation = 10, DDR = 0, P54 = 0		60.7		
		Decimation = 10, DDR = 1, P54 = 0		52.7		
		Decimation = 16, DDR = 0, P54 = 0		60.7		
		Decimation = 16, DDR = 0, P54 = 1		51.5		
		Decimation = 16, DDR = 1, P54 = 0		52.7		
		Decimation = 16, DDR = 1, P54 = 1		43.9		
		Decimation = 20, DDR = 0, P54 = 0		60.7		
		Decimation = 20, DDR = 1, P54 = 0		52.7		
		Decimation = 32, DDR = 0, P54 = 0		60.7		
		Decimation = 32, DDR = 0, P54 = 1		51.5		
		Decimation = 32, DDR = 1, P54 = 0		52.7		
$t_{su(SYNC\sim F)}$	SYNC~ to LMFC setup time(3) Required SYNC~ setup time relative to the internal LMFC boundary.			40		$t_{(DEVCLK)}$
$t_{h(SYNC\sim F)}$	SYNC~ to LMFC hold time(3) Required SYNC~ hold time relative to the internal LMFC boundary.			–8		
$t_{(SYNC\sim)}$	SYNC~ assertion time Required SYNC~ assertion time before deassertion to initiate a link resynchronization.			4		Frame clock cycles
$t_{d(LMFC)}$	Delay from SYSREF sampled high by DEVCLK to internal LMFC boundary			40		$t_{(DEVCLK)}$
$t_{(ILA)}$	Duration of initial lane alignment sequence			4		Multi-frame clock cycles
SYSREF						
$t_{su(SYS)}$	Setup time SYSREF relative to DEVCLK rising edge(4)			40		ps
$t_{h(SYS)}$	Hold time SYSREF relative to DEVCLK rising edge(4)			40		ps
$t_{(PH\_SYS)}$	SYSREF assertion duration after rising edge event.		8			$t_{(DEVCLK)}$
$t_{(PL\_SYS)}$	SYSREF deassertion duration after falling edge event.		8			$t_{(DEVCLK)}$
$t_{(SYS)}$	Period SYSREF±	DDR = 0, P54 = 0		K × F × 10		$t_{(DEVCLK)}$
		DDR = 0, P54 = 1		K × F × 8		
		DDR = 1, P54 = 0		K × F × 5		
		DDR = 1, P54 = 1		K × F × 4		

(2) The values given are functional delays only. Additional propagation delay of 0 to 3 clock cycles will be present.
(3) This parameter must be met to achieve deterministic alignment of the data frame and NCO phase to other similar devices. If this parameter is not met the device will still function correctly but will not be aligned to other devices.
(4) This parameter is specified by design, characterization, or both and is not tested in production.

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Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
SERIAL INTERFACE (REFER TO Figure 2)					
$f_{(SCK)}$	Serial clock frequency(5)			20	MHz
$t_{(PH)}$	Serial clock high time	20			ns
$t_{(PL)}$	Serial clock low time	20			ns
t_{su}	Serial-data to serial-clock rising setup time(5)	10			ns
t_h	Serial-data to serial clock rising hold time(5)	10			ns
$t_{(CSS)}$	$\overline{SCS}$-to-serial clock rising setup time	10			ns
$t_{(CSH)}$	$\overline{SCS}$-to-serial clock falling hold time	10			ns
$t_{(IAG)}$	Inter-access gap	10			ns

(5) This parameter is specified by design and is not tested in production.

6.7 Internal Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DEVICE (SAMPLING) CLOCK						
$t_{d(A)}$	Sampling (aperture) delay	Input CLK transition to sampling instant		0.64		ns
$t_{(AJ)}$	Aperture jitter			0.1		ps RMS
$t_{(LAT)}$	ADC core latency. See (1)	Decimation = 1, DDR = 1, P54 = 0		64		$t_{(DEVCLK)}$
CALIBRATION TIMING CHARACTERISTICS (REFER TO THE *CALIBRATION* SECTION)						
$t_{(CAL)}$	Calibration cycle time	Calibration = FG, T_AUTO=1			227×10^6	$t_{(DEVCLK)}$
		Calibration = FG, T_AUTO=0			102×10^6	
JESD204B INTERFACE LINK TIMING CHARACTERISTICS (REFER TO Figure 1)						
$t_{d(LMFC)}$	SYSREF to LMFC delay Functional delay between SYSREF assertion latched and LMFC frame boundary(1)	All decimation modes		40		$t_{(DEVCLK)}$
$t_{d(TX)}$	LMFC to Frame Boundary delay - DDC Bypass Mode Functional delay from LMFC frame boundary to beginning of next multi-frame in transmitted data(2)	Decimation = 1, DDR = 1, P54 = 0		52.7		$t_{(DEVCLK)}$
$t_{d(TX)}$	LMFC to frame boundary delay - decimation modes Functional delay from LMFC frame boundary to beginning of next multi-frame in transmitted data(2)	Decimation = 4, DDR = 1, P54 = 0		52.7		$t_{(DEVCLK)}$
		Decimation = 4, DDR = 1, P54 = 1		43.9		
		Decimation = 8, DDR = 0, P54 = 0		60.7		
		Decimation = 8, DDR = 0, P54 = 1		51.5		
		Decimation = 8, DDR = 1, P54 = 0		52.7		
		Decimation = 8, DDR = 1, P54 = 1		43.9		
		Decimation = 10, DDR = 0, P54 = 0		60.7		
		Decimation = 10, DDR = 1, P54 = 0		52.7		
		Decimation = 16, DDR = 0, P54 = 0		60.7		
		Decimation = 16, DDR = 0, P54 = 1		51.5		
		Decimation = 16, DDR = 1, P54 = 0		52.7		
		Decimation = 16, DDR = 1, P54 = 1		43.9		
		Decimation = 20, DDR = 0, P54 = 0		60.7		
		Decimation = 20, DDR = 1, P54 = 0		52.7		
		Decimation = 32, DDR = 0, P54 = 0		60.7		
		Decimation = 32, DDR = 0, P54 = 1		51.5		
		Decimation = 32, DDR = 1, P54 = 0		52.7		
$t_{d(LMFC)}$	Delay from SYSREF sampled high by DEVCLK to internal LMFC boundary			40		$t_{(DEVCLK)}$
$t_{(ILA)}$	Duration of initial lane alignment sequence			4		Multi-frame clock cycles

(1) Unless otherwise specified, delays quoted are exact un-rounded functional delays (assuming zero propagation delay).
(2) The values given are functional delays only. Additional propagation delay of 0 to 3 clock cycles will be present.

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6.8 Switching Characteristics

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground mode calibration with timing calibration enabled. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL DATA OUTPUTS						
	Serialized output bit rate		1		10	Gbps
	Serialized output bit rate	DDR = 0, P54 = 0		f_S		
		DDR = 0, P54 = 1		1.25 × f_S		
		DDR = 1, P54 = 0		2 × f_S		
		DDR = 1, P54 = 1		2.5 × f_S		
t_{TLH}	LH transition time — differential	10% to 90%, 8 Gbps		35		ps
t_{THL}	HL transition time — differential	10% to 90%, 8 Gbps		35		ps
UI	Unit interval	8 Gbps serial rate		125		ps
DDJ	Data dependent jitter	8 Gbps serial rate		11.3		ps
RJ	Random Jitter	8 Gbps serial rate		1.4		ps
SERIAL INTERFACE						
$t_{(OZD)}$	SDO tri-state to driven	See Figure 2			5	ns
$t_{(ODZ)}$	SDO driven to tri-state		2.5		5	ns
$t_{(OD)}$	SDO output delay				20	ns

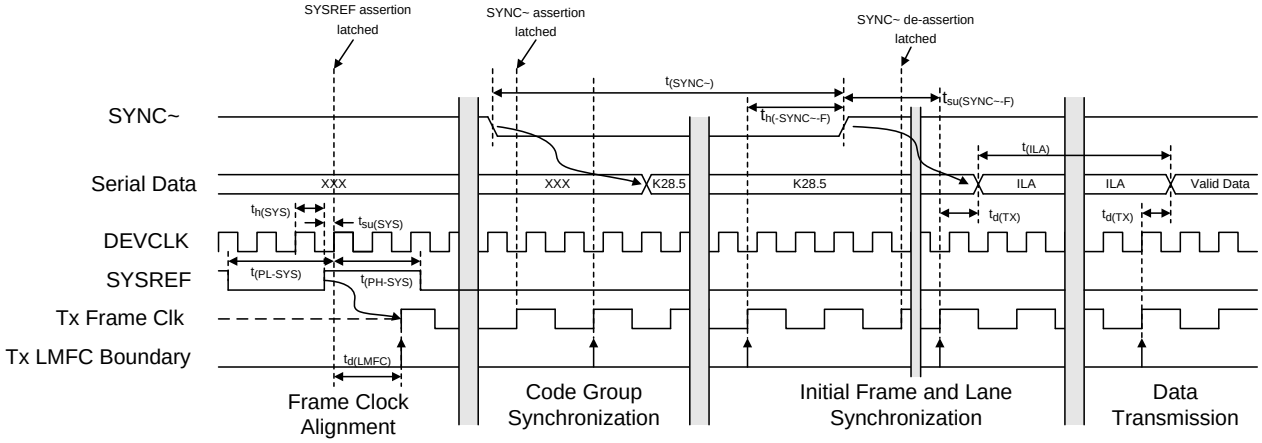

Figure 1. JESD204 Synchronization

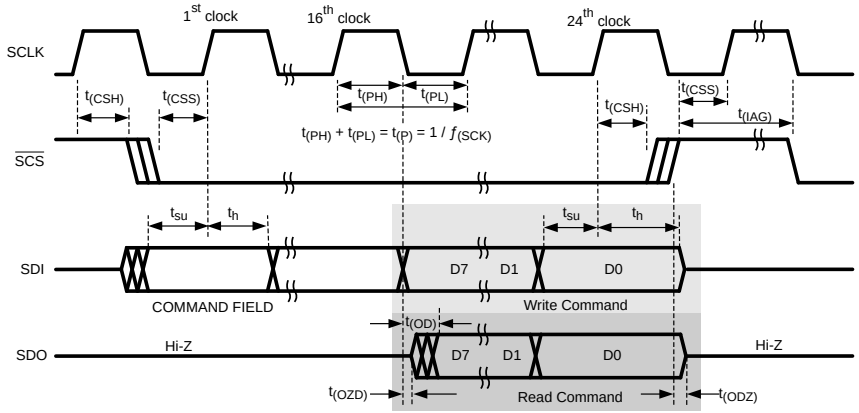

Figure 2. Serial Interface Timing

6.9 Typical Characteristics

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. T_A = 25°C. V_I = –1 dBFS.

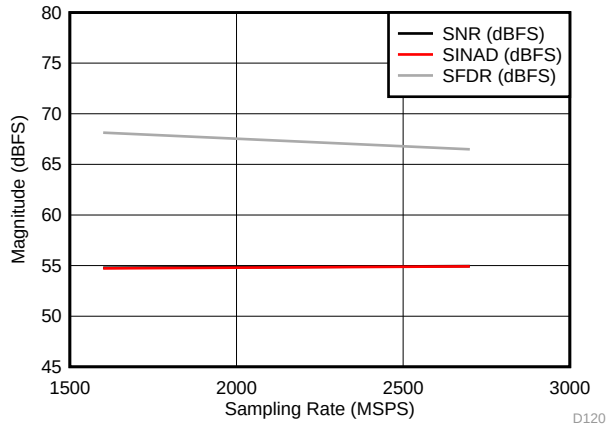

Figure 3. SNR, SINAD, SFDR vs Sampling Rate

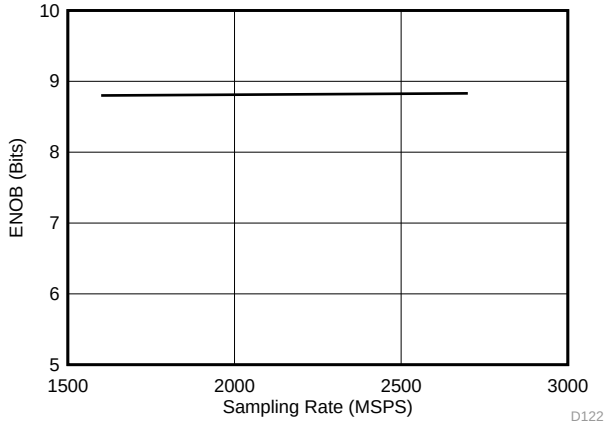

Figure 4. ENOB vs Sampling Rate

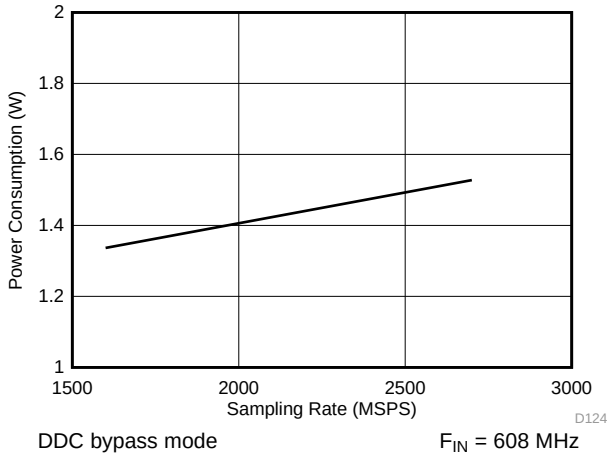

Figure 5. Power Consumption vs Sampling Rate

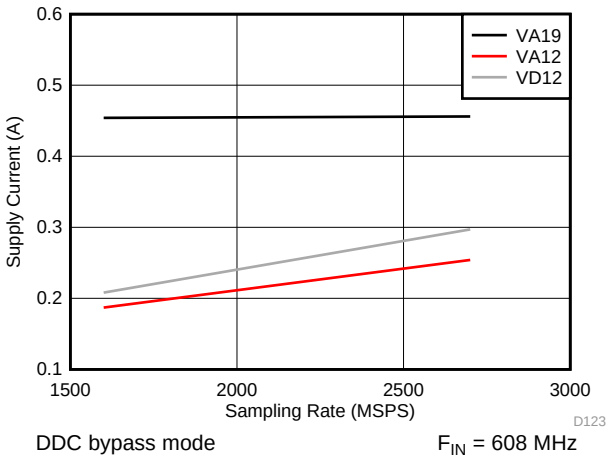

Figure 6. Supply Current vs Sampling Rate

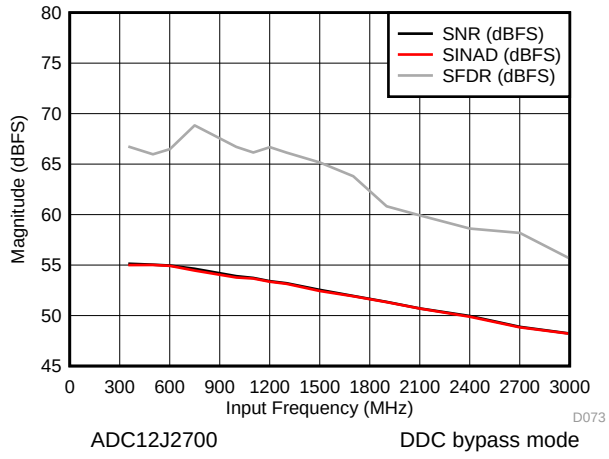

Figure 7. SNR, SINAD, SFDR vs Input Frequency

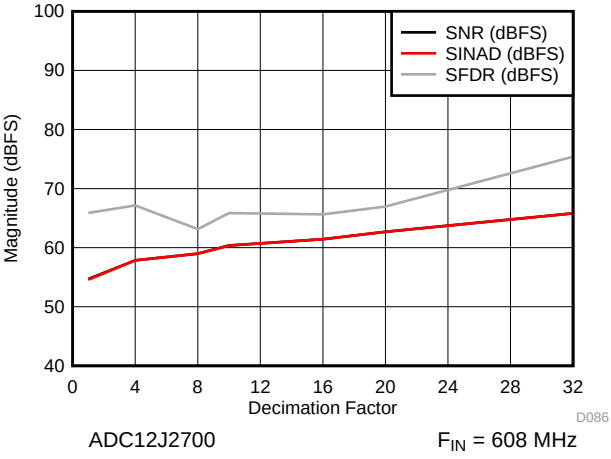

Figure 8. SNR, SINAD, SFDR vs Decimation Setting

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Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. T_A = 25°C. V_I = –1 dBFS.

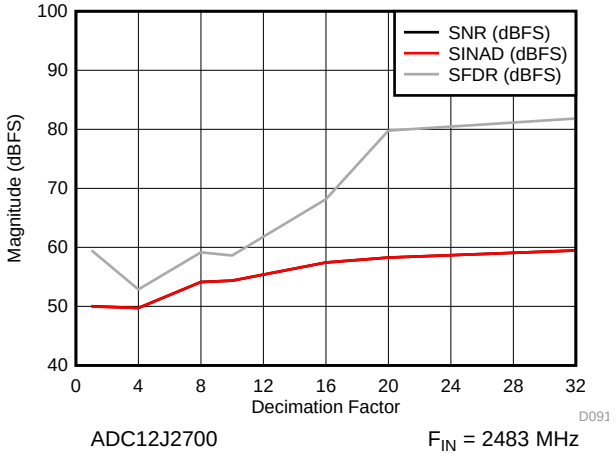

Figure 9. SNR, SINAD, SFDR vs Decimation Setting

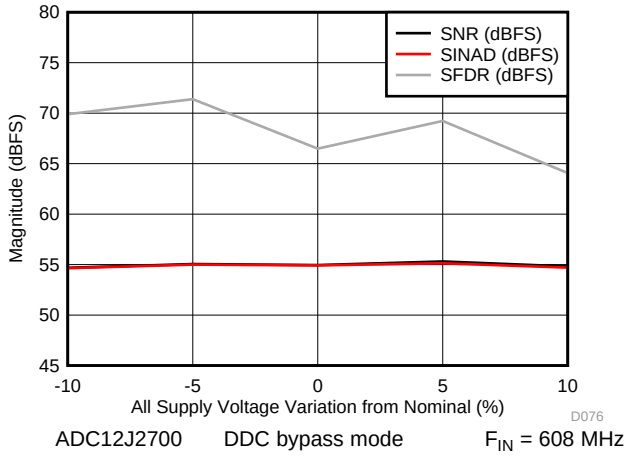

Figure 10. SNR, SINAD, SFDR vs Supply Voltage

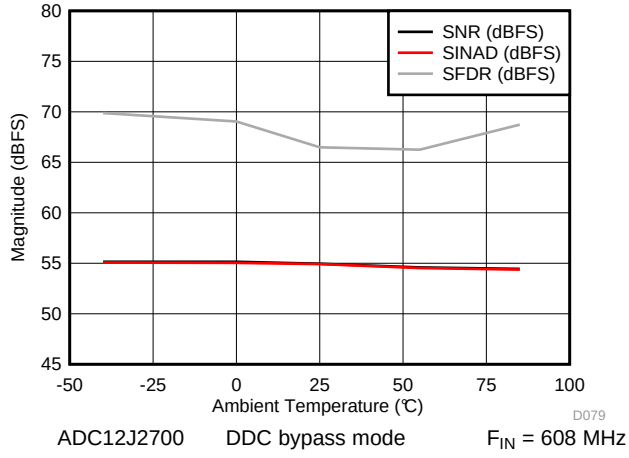

Figure 11. SNR, SINAD, SFDR vs Temperature

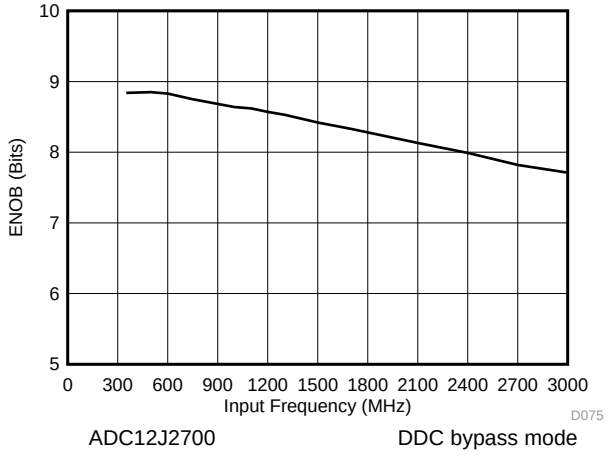

Figure 12. ENOB vs Input Frequency

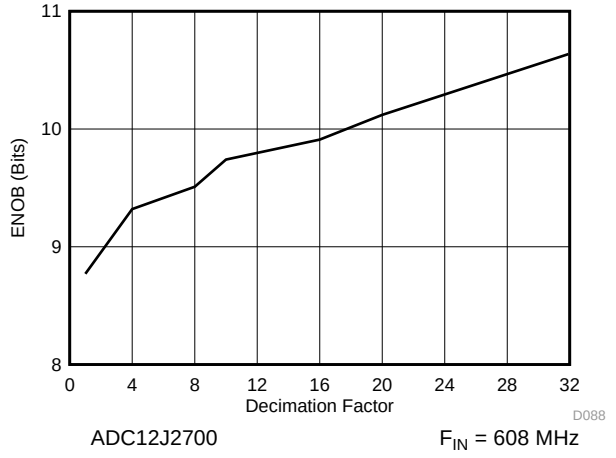

Figure 13. ENOB vs Decimation Setting

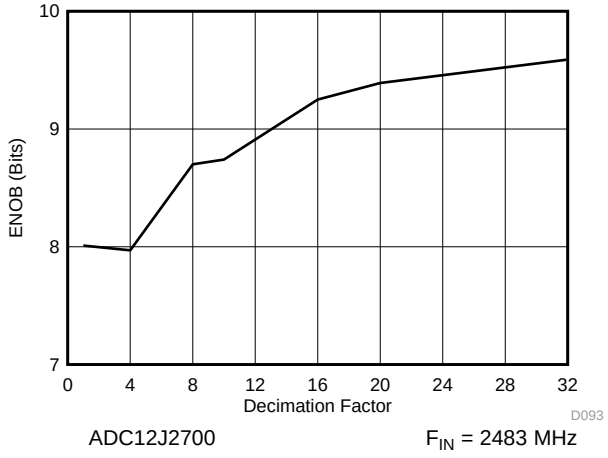

Figure 14. ENOB vs Decimation Setting

Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. T_A = 25°C. V_I = –1 dBFS.

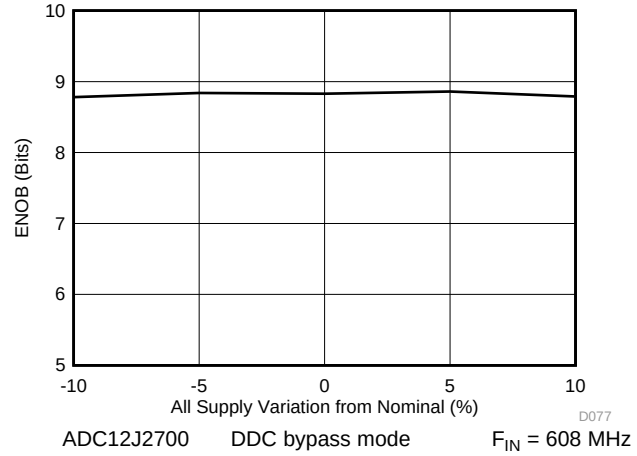

Figure 15. ENOB vs Supply Voltage

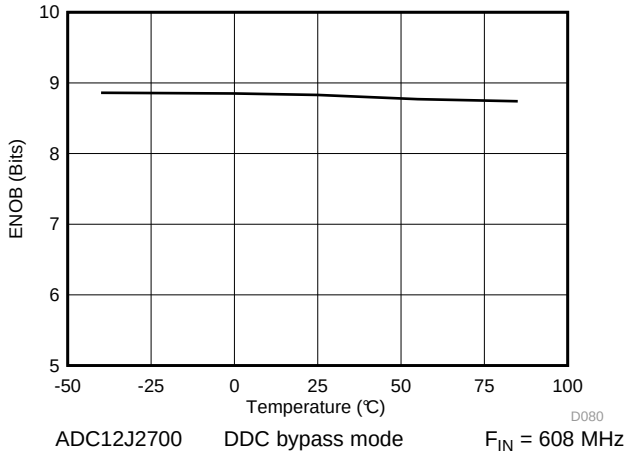

Figure 16. ENOB vs Temperature ADC12J2700

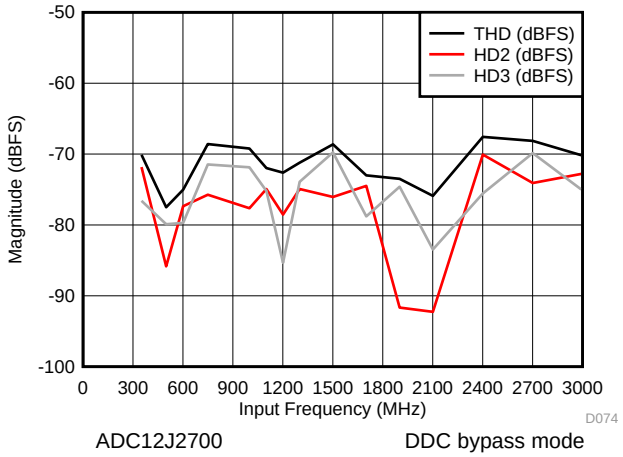

Figure 17. THD, H2, H3 vs Input Frequency

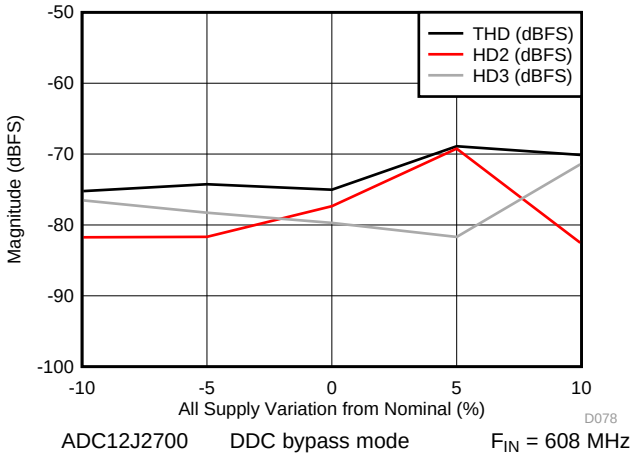

Figure 18. THD, H2, H3 vs Supply Voltage

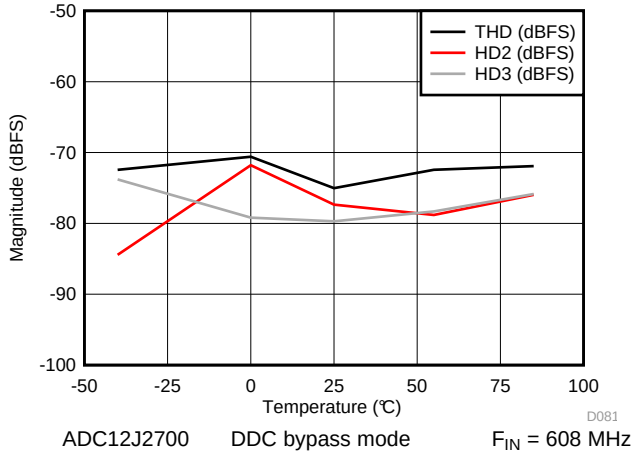

Figure 19. THD, H2, H3 vs Temperature

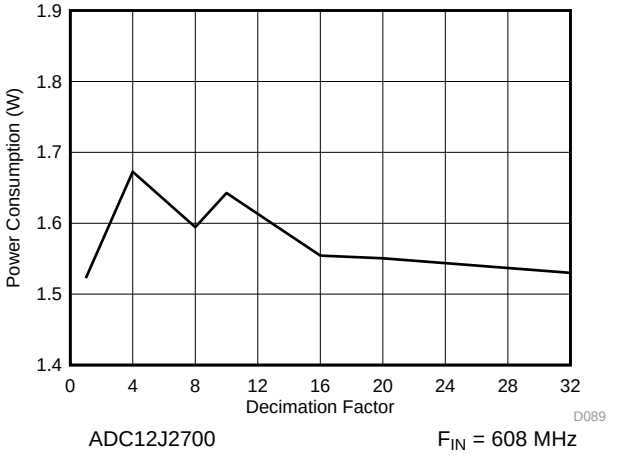

Figure 20. Power Consumption vs Decimation Setting

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Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. T_A = 25°C. V_I = –1 dBFS.

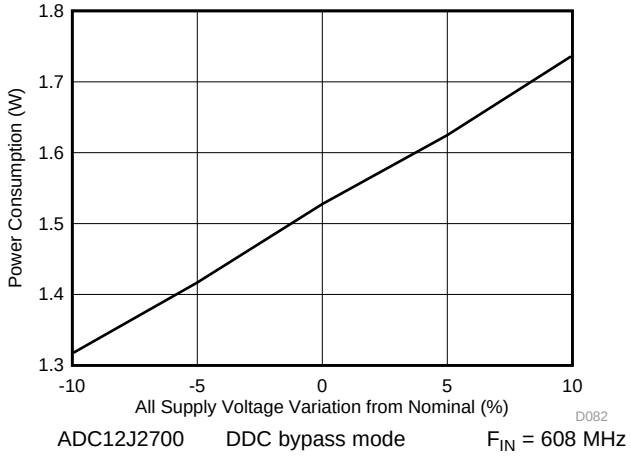

Figure 21. Power Consumption vs Supply Voltage

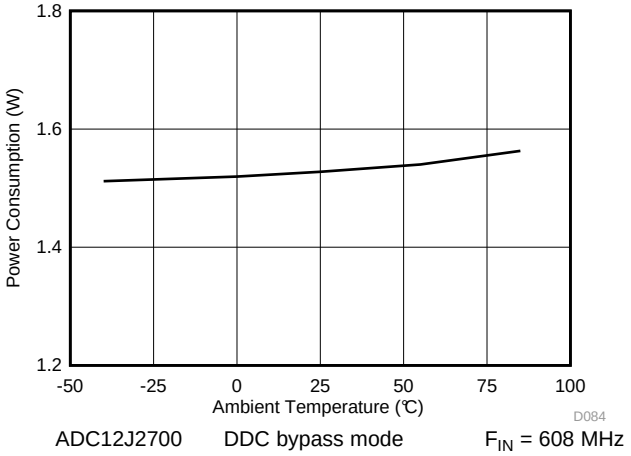

Figure 22. Power Consumption vs Temperature

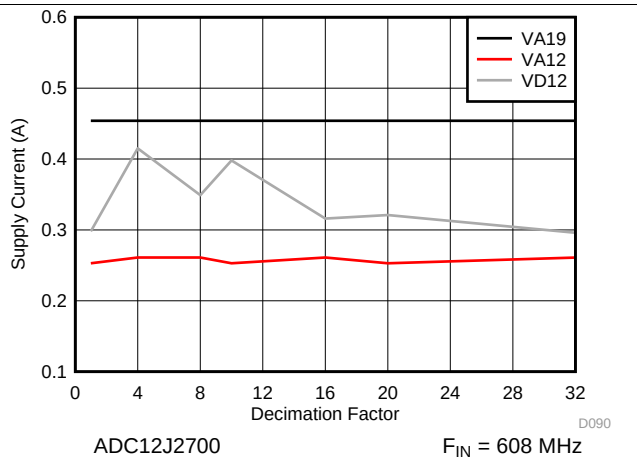

Figure 23. Supply Current vs Decimation Setting

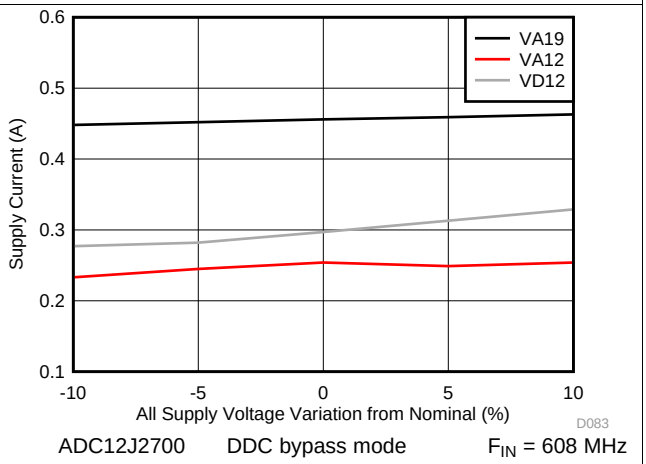

Figure 24. Supply Current vs Supply Voltage

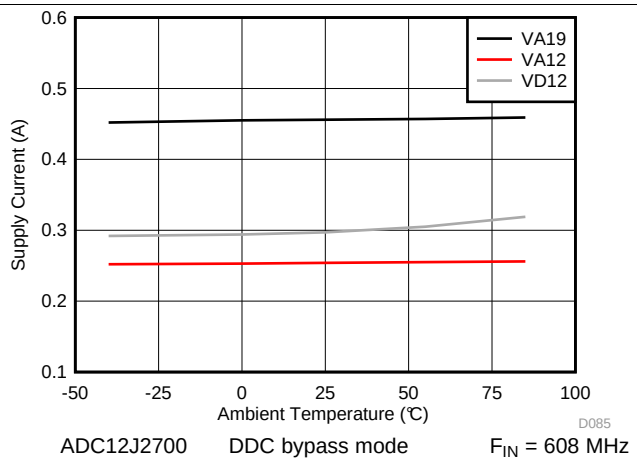

Figure 25. Supply Current vs Temperature

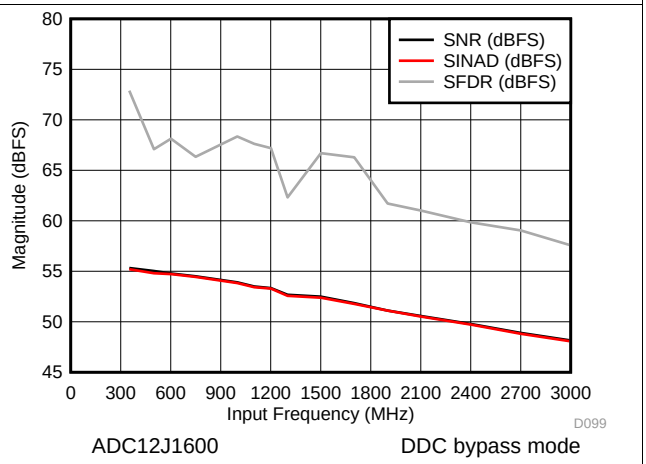

Figure 26. SNR, SINAD, SFDR vs Input Frequency

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Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. T_A = 25°C. V_I = –1 dBFS.

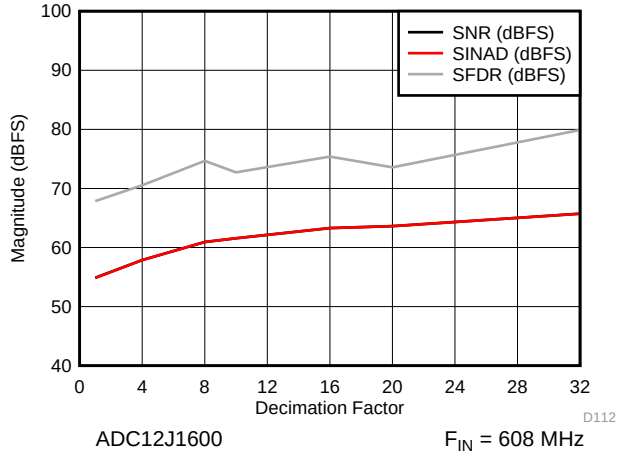

Figure 27. SNR, SINAD, SFDR vs Decimation Setting

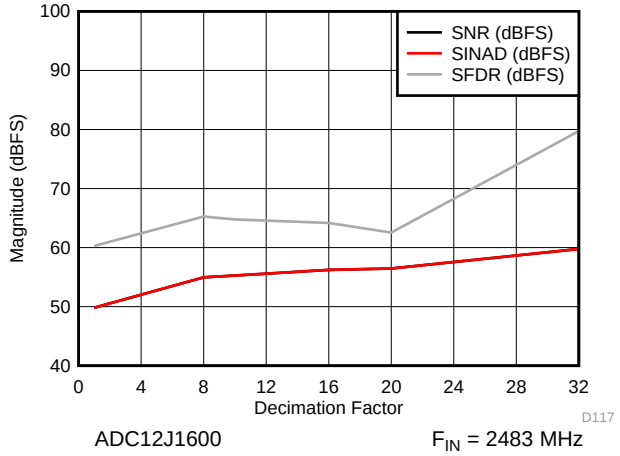

Figure 28. SNR, SINAD, SFDR vs Decimation Setting

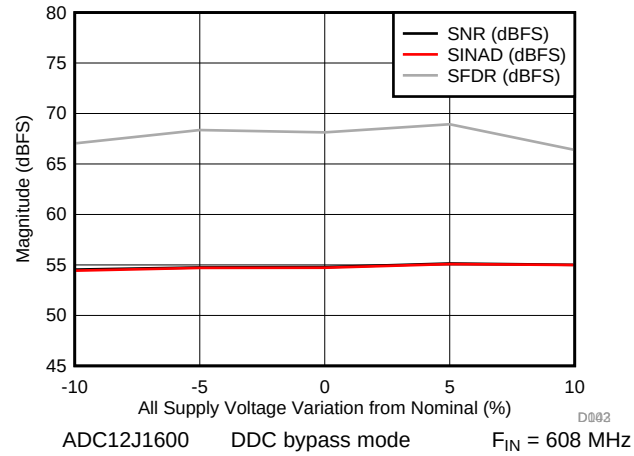

Figure 29. SNR, SINAD, SFDR vs Supply Voltage

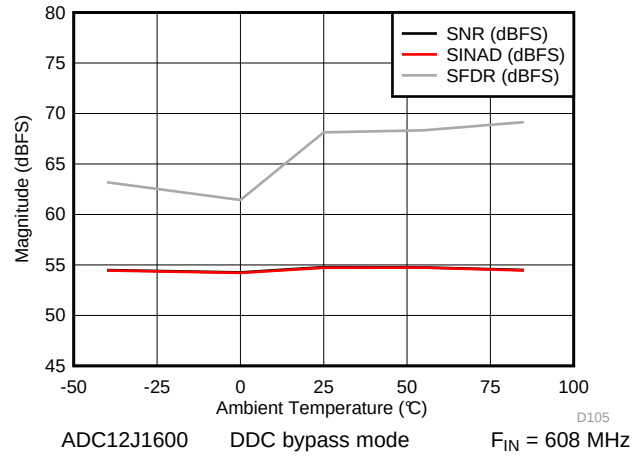

Figure 30. SNR, SINAD, SFDR vs Temperature

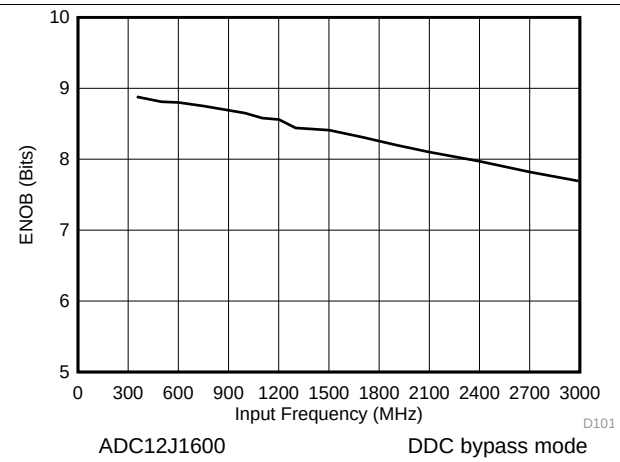

Figure 31. ENOB vs Input Frequency

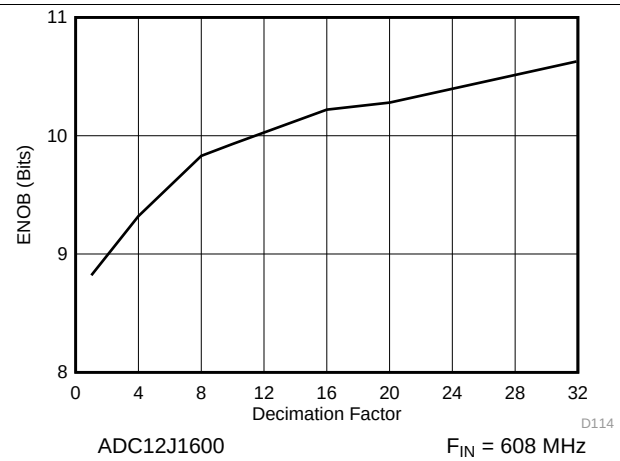

Figure 32. ENOB vs Decimation Setting

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Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. T_A = 25°C. V_I = –1 dBFS.

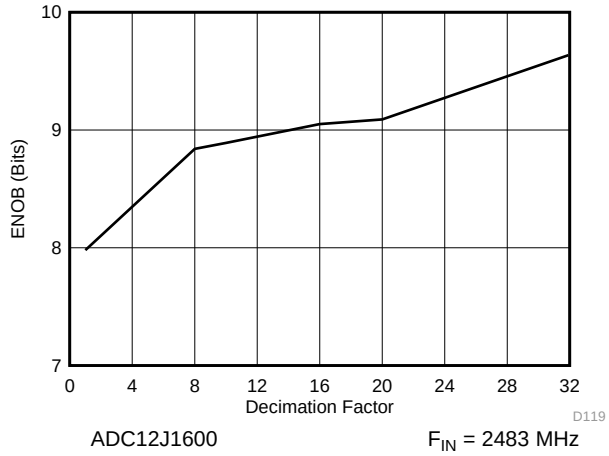

Figure 33. ENOB vs Decimation Setting

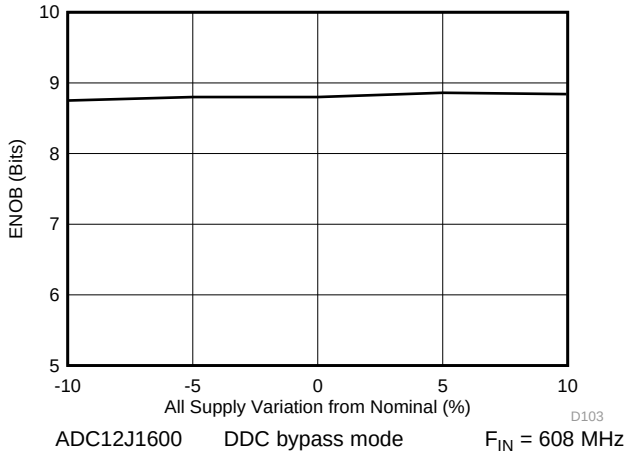

Figure 34. ENOB vs Supply Voltage

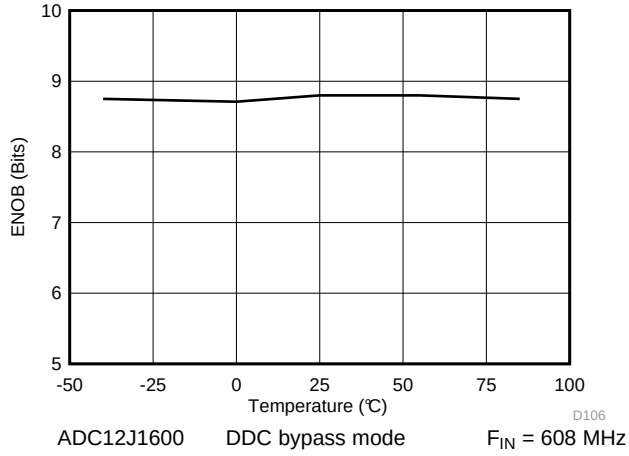

Figure 35. ENOB vs Temperature

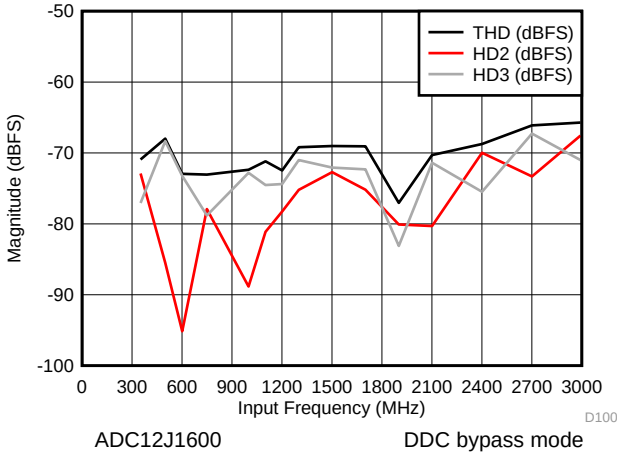

Figure 36. THD, H2, H3 vs Input Frequency

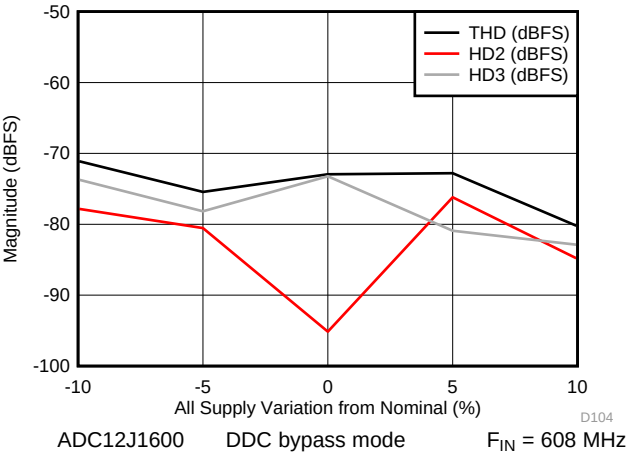

Figure 37. THD, H2, H3 vs Supply Voltage

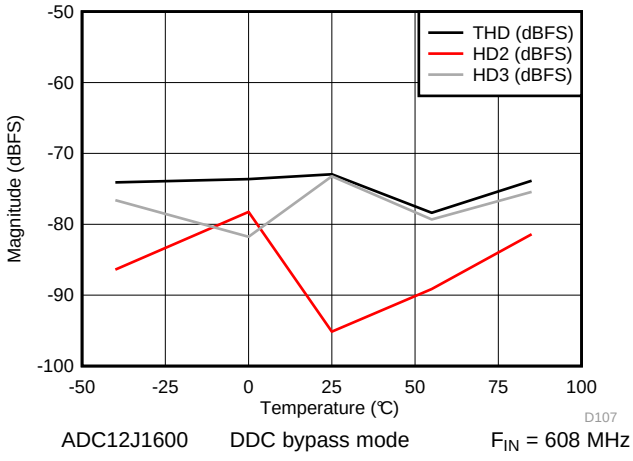

Figure 38. THD, H2, H3 vs Temperature

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Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. T_A = 25°C. V_I = –1 dBFS.

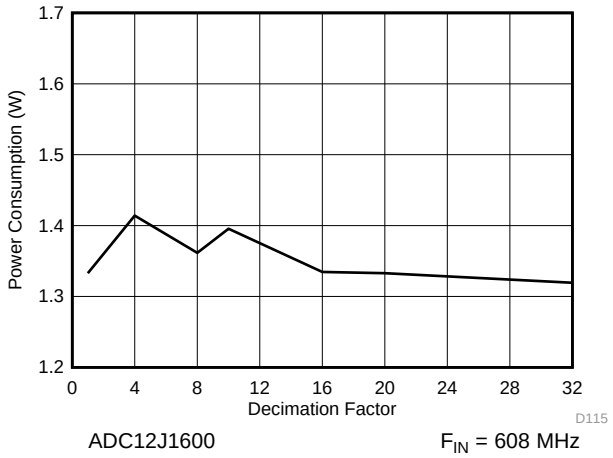

Figure 39. Power Consumption vs Decimation Setting

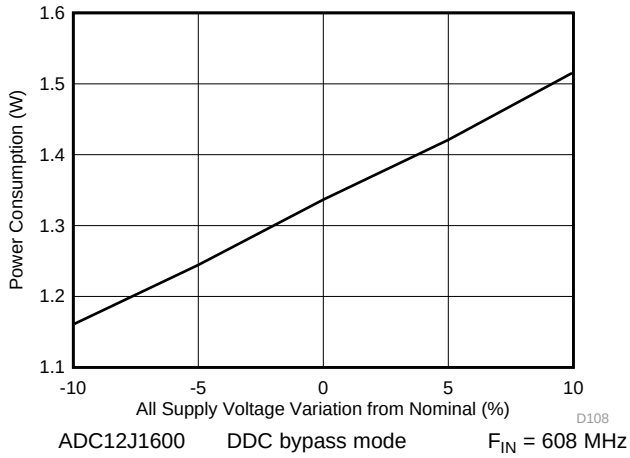

Figure 40. Power Consumption vs Supply Voltage

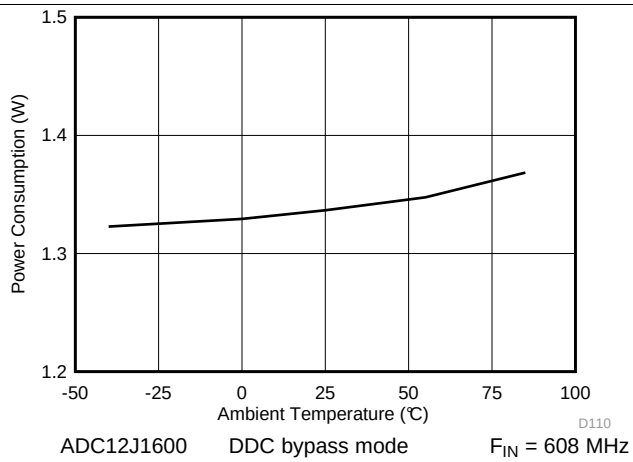

Figure 41. Power Consumption vs Temperature

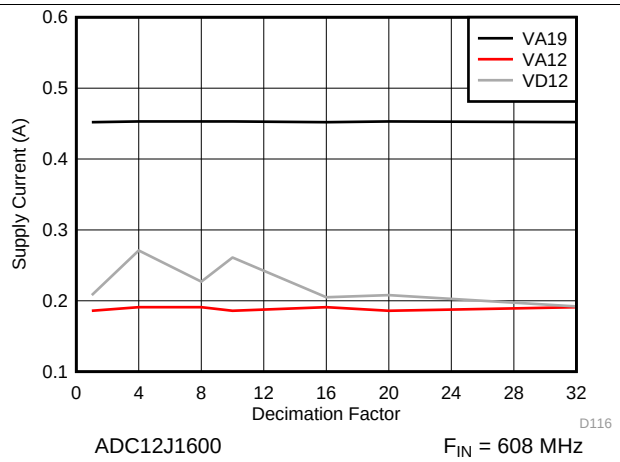

Figure 42. Supply Current vs Decimation Setting

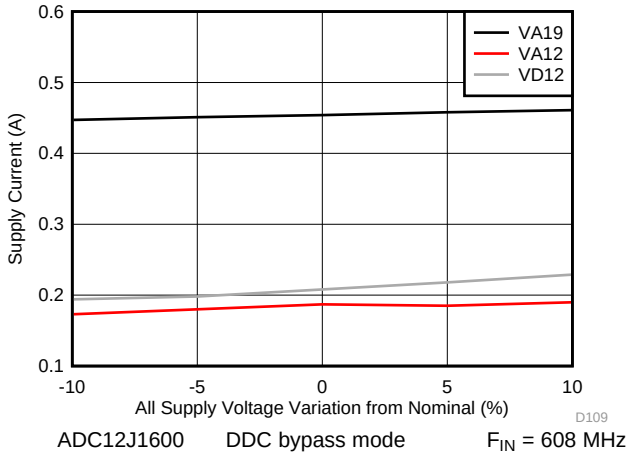

Figure 43. Supply Current vs Supply Voltage

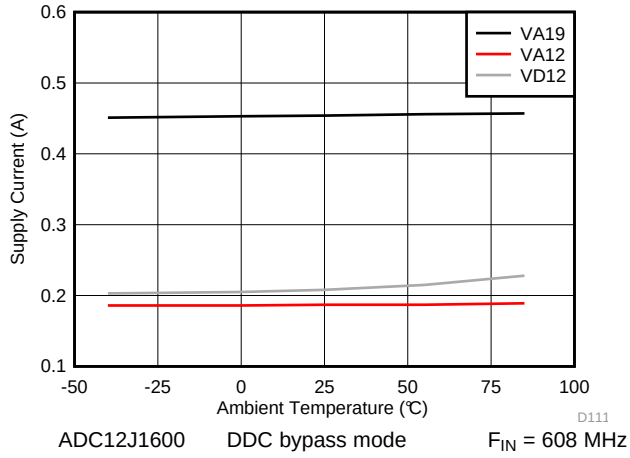

Figure 44. Supply Current vs Temperature

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Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. T_A = 25°C. V_I = –1 dBFS.

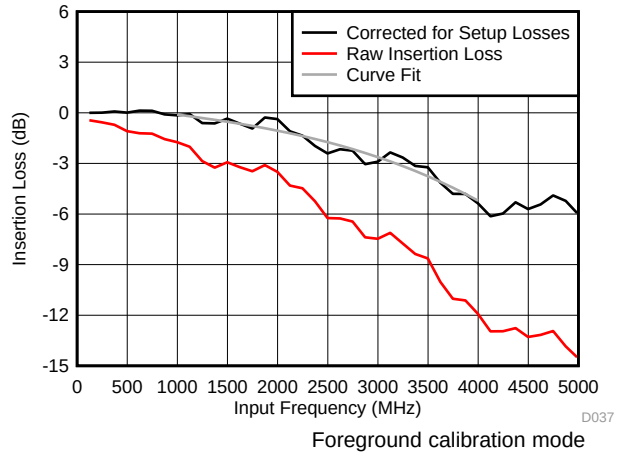

Figure 45. Insertion Loss vs Input Frequency

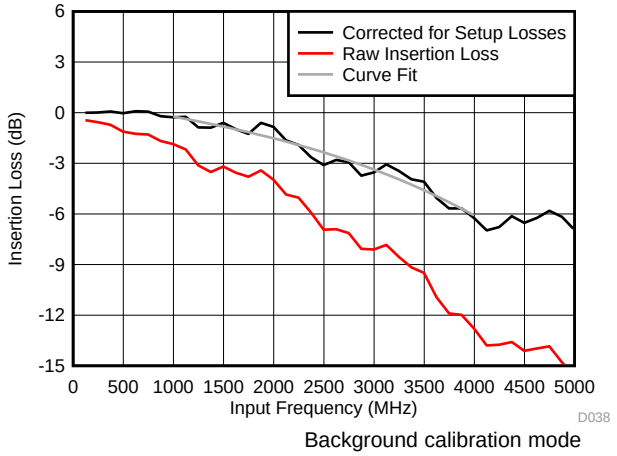

Figure 46. Insertion Loss vs Input Frequency

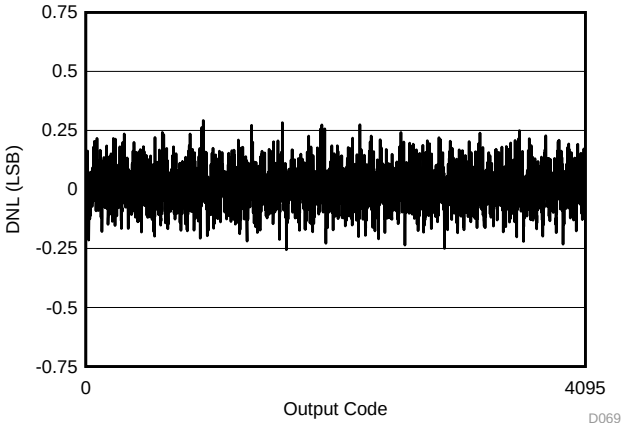

Figure 47. DNL versus Code - ADC12J2700

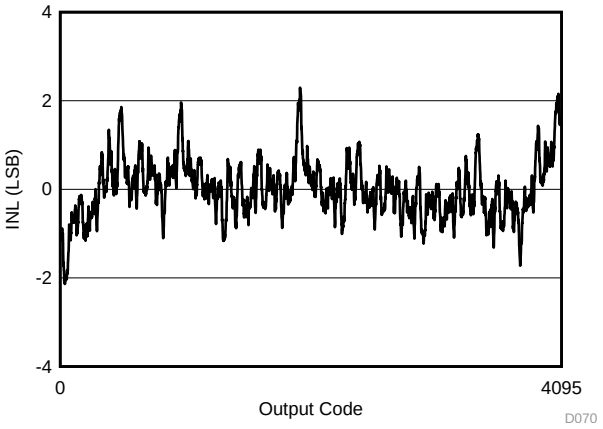

Figure 48. INL versus Code - ADC12J2700

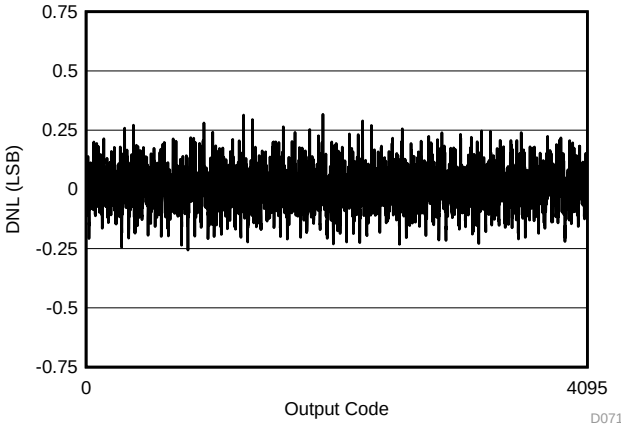

Figure 49. DNL versus Code - ADC12J1600

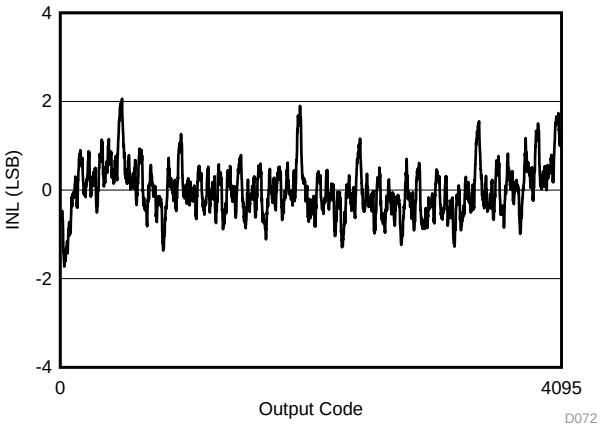

Figure 50. INL versus Code - ADC12J1600

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Typical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN FSR (AC coupled) = Default setting, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 2.7 or 1.6 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a Foreground mode calibration with Timing Calibration enabled. T_A = 25°C. V_I = –1 dBFS.

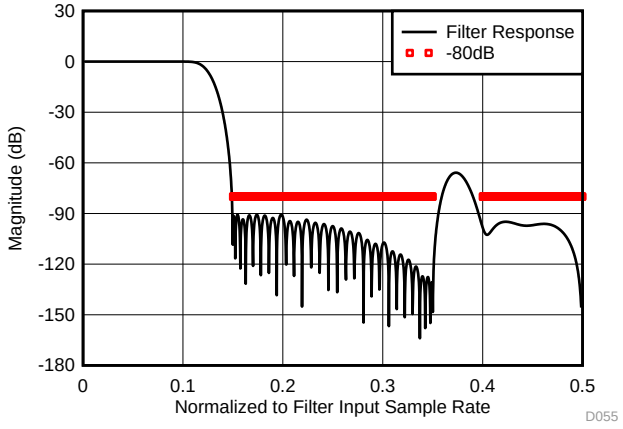

Figure 51. Decimate by 4 - Stopband Response

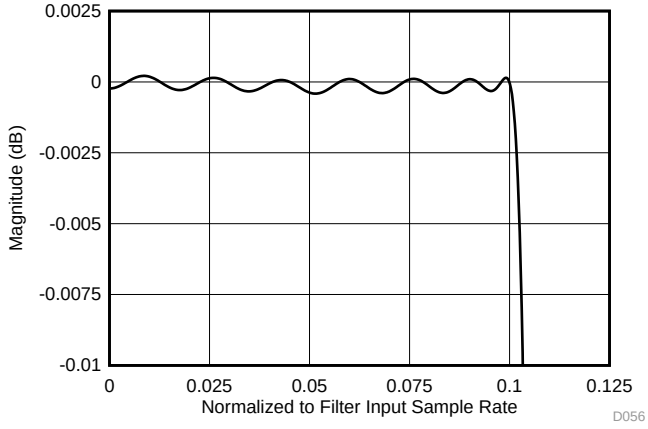

Figure 52. Decimate by 4 - Passband Response

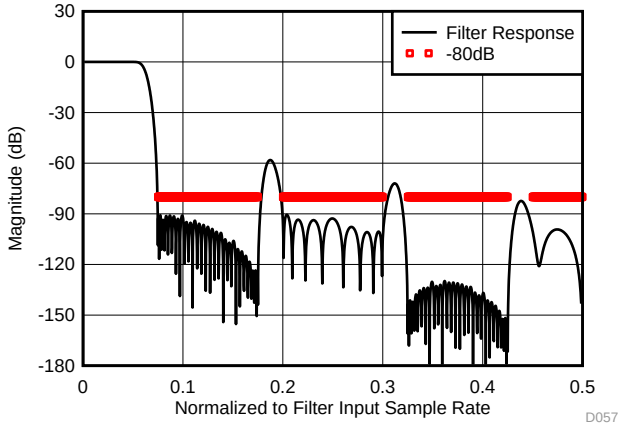

Figure 53. Decimate by 8 - Stopband Response

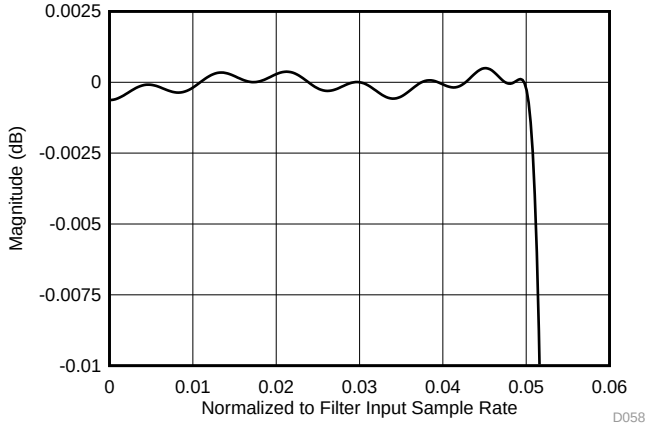

Figure 54. Decimate by 8 - Passband Response

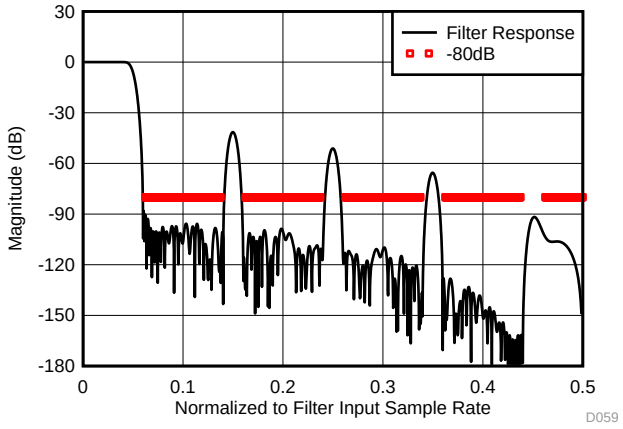

Figure 55. Decimate by 10 - Stopband Response

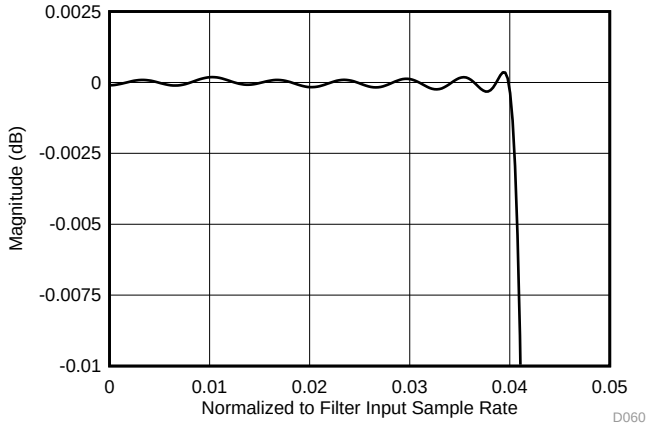

Figure 56. Decimate by 10 - Passband Response

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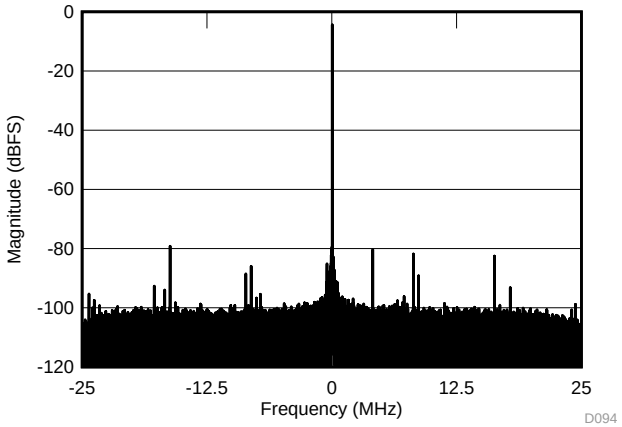
DDC Bypass Mode f_S = 1600 MSPS
F_{IN} = 2497.97 MHz at –1 dBFS

Figure 110. Spectrum — DDC Bypass Mode



f_S = 1600 MSPS $f_{(NCO)}$ = 2500 MHz
F_{IN} = 2497.97 MHz at –1 dBFS

Figure 111. Spectrum — Decimate-by-32

8.2.2 Oscilloscope

The ADC12J1600 and ADC12J2700 devices are equally well-suited for high-speed time-domain applications such as oscilloscopes. The following typical application is for a generic high-speed oscilloscope. Adjustable gain is provided by the front-end resistor ladder and selection mux, and the gain adjustments of the LMH6518 device. Additional gain fine-tuning can be achieved using the full-scale range adjustment features of the ADC.

Figure 112. Simplified Schematic for an Oscilloscope

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8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 88.

Table 88. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Maximum sample rate	1600 MSPS
Maximum input frequency	1500 MHz
1-dB flat-frequency range	0 to 1000 MHz
Signal maximum amplitude	6 dBm
Signal minimum amplitude	48 dBc
Maximum capture depth	1 million points

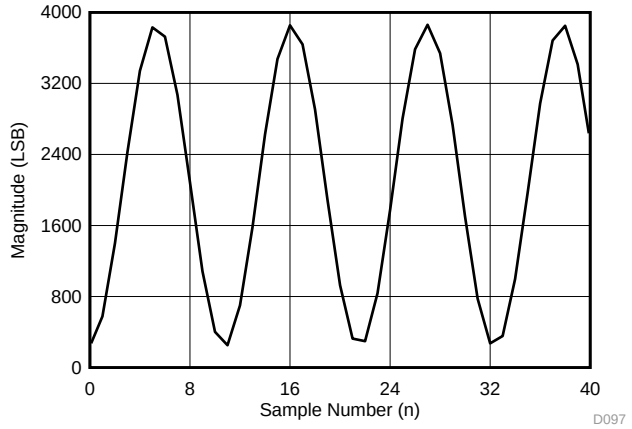
8.2.2.2 Detailed Design Procedure

Use the following primary steps to design a 12-bit oscilloscope:

- Select the desired sampling rate based on the maximum sampling-rate requirement.
- Select the input path components (LNA, amplifier, and other components) based on the maximum input frequency and 1-dB flat-frequency range requirements.
- Set the attenuation range steps based on the required minimum and maximum values for the signal amplitude.
- Select the memory size based on the resolution of the ADC output (12 bits) and the required maximum number of sample points.

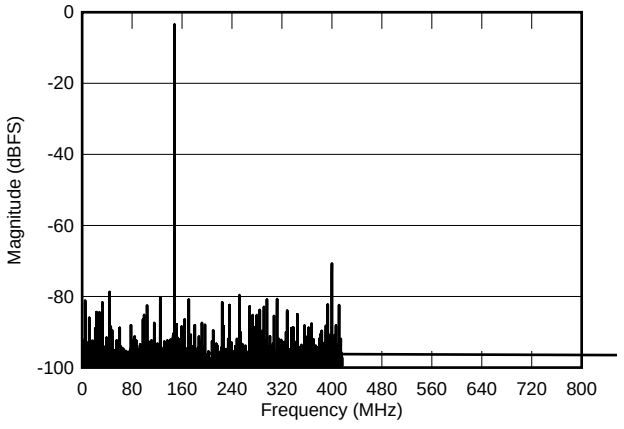
8.2.2.3 Application Curves

The following curves show the time-domain sample data for a 150-MHz input signal at –1 dBFS, sampled at 1600 MSPS using the ADC12J1600 device. Figure 113 shows the raw time-domain data. Figure 114 shows the spectrum of the captured signal which shows the additional capability of a 12-bit ADC oscilloscope to provide basic spectrum-analysis functions with reasonable performance.



F_{IN} = 147.97 MHz at –1 dBFS f_S = 1600 MSPS

Figure 113. Raw Time-Domain Data



F_{IN} = 147.97 MHz at –1 dBFS f_S = 1600 MSPS

Figure 114. Captured Signal Spectrum

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8.3 Initialization Set-Up

8.3.1 JESD204B Startup Sequence

The JESD204B interface requires a specific startup and alignment sequence. The general order of that sequence is listed in the following steps.

1. Power up or reset the ADC12J1600 and ADC12J2700 devices.
2. Program JESD_EN = 0 to shut down the link and enable configuration changes.
3. Program DECIMATE, SCRAM_EN, KM1 and DDR to the desired settings.
4. Configure the device calibration settings as desired, and initiate a calibration (set CAL_SFT = 1).
5. Program JESD_EN = 1 to enable the link.
6. Apply at least one SYSREF rising edge to establish the LMFC phase.
7. Assert SYNC~ from the data receiver to initiate link communications.
8. After the JESD204B receiver has established code group synchronization, SYNC~ is de-asserted and the ILA process begins.
9. Immediately following the end of the ILA sequence normal data output begins.

NOTE

If deterministic latency is not required this step can be omitted.

8.4 Dos and Don'ts

8.4.1 Common Application Pitfalls

Driving the inputs (analog or digital) beyond the power supply rails. For device reliability, an input must not go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits even on a transient basis can cause faulty, or erratic, operation and can impair device reliability. High-speed digital circuits exhibiting undershoot that goes more than a volt below ground is common. To control overshoot, the impedance of high-speed lines must be controlled and these lines must be terminated in the characteristic impedance.

Care must be taken not to overdrive the inputs of the ADC12J1600 and ADC12J2700 devices. Such practice can lead to conversion inaccuracies and even to device damage.

Incorrect analog input common-mode voltage in the DC-coupled mode. As described in the *The Analog Inputs* and *DC Coupled Input Usage* sections, the input common-mode voltage (V_{CMI}) must remain the specified range as referenced to the VCMO pin, which has a variability with temperature that must also be tracked. Distortion performance is degraded if the input common mode voltage is outside the specified V_{CMI} range.

Using an inadequate amplifier to drive the analog input. Use care when choosing a high frequency amplifier to drive the ADC12J1600 and ADC12J2700 devices because many high-speed amplifiers have higher distortion than the ADC12J1600 and ADC12J2700 devices which results in overall system performance degradation.

Driving the clock input with an excessively high level signal. The ADC input clock level must not exceed the level described in the *Recommended Operating Conditions* table because the input offset can change if these levels are exceeded.

Inadequate input clock levels. As described in the *Using the Serial Interface* section, insufficient input clock levels can result in poor performance. Excessive input-clock levels can result in the introduction of an input offset.

Using a clock source with excessive jitter, using an excessively long input clock signal trace, or having other signals coupled to the input clock signal trace. These pitfalls cause the sampling interval to vary which causes excessive output noise and a reduction in SNR performance.

Failure to provide adequate heat removal. As described in the *Thermal Management* section, providing adequate heat removal is important to ensure device reliability. Adequate heat removal is primarily provided by properly connecting the thermal pad to the circuit board ground planes. Multiple vias should be arranged in a grid pattern in the area of the thermal pad. These vias will connect the topside pad to the internal ground planes and to a copper pour area on the opposite side of the printed circuit board.

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9 Power Supply Recommendations

Data-converter-based systems draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 10-µF capacitor must be placed within one inch (2.5 cm) of the device power pins for each supply voltage. A 0.1-µF capacitor must be placed as close as possible to each supply pin, preferably within 0.5 cm. Leadless chip capacitors are preferred due to their low-lead inductance.

As is the case with all high-speed converters, the ADC12J1600 and ADC12J2700 devices must be assumed to have little power-supply noise-rejection. Any power supply used for digital circuitry in a system where a large amount of digital power is consumed must not be used to supply power to the ADC12J1600 and ADC12J2700 devices. If not a dedicated supply, the ADC supplies must be the same supply used for other analog circuitry.

9.1 Supply Voltage

The ADC12J1600 and ADC12J2700 devices are specified to operate with nominal supply voltages of 1.9 V (VA19) and 1.2 V (VA12, VD12). For detailed information regarding the operating voltage minimums and maximums see the *Recommended Operating Conditions* table.

During power-up the voltage on all 1.9-V supplies must always be equal to or greater than the voltage on the 1.2-V supplies. Similarly, during power-down, the voltage on the 1.2-V supplies must always be lower than or equal to that of the 1.9-V supplies. In general, supplying all 1.9-V buses from a single regulator, and all 1.2-V buses from a single regulator is the easiest method to ensure that the 1.9-V supplies are greater than the 1.2-V supplies. If the 1.2-V buses are generated from separate regulators, they must rise and fall together (within 200 mV).

The voltage on a pin, including a transient basis, must not have a voltage that is in excess of the supply voltage or below ground by more than 150 mV. A pin voltage that is higher than the supply or that is below ground can be a problem during startup and shutdown of power. Ensure that the supplies to circuits driving any of the input pins, analog or digital, do not rise faster than the voltage at the ADC12J1600 and ADC12J2700 power pins.

The values in the *Absolute Maximum Ratings* table must be strictly observed including during power up and power down. A power supply that produces a voltage spike at power turnon, turnoff, or both can destroy the ADC12J1600 and ADC12J2700 devices. Many linear regulators produce output spiking at power on unless there is a minimum load provided. Active devices draw very little current until the supply voltages reach a few hundred millivolts. The result can be a turn-on spike that destroys the ADC12J1600 and ADC12J2700 devices, unless a minimum load is provided for the supply. A 100-Ω resistor at the regulator output provides a minimum output current during power up to ensure that no turn-on spiking occurs. Whether a linear or switching regulator is used, TI recommends using a soft-start circuit to prevent overshoot of the supply.

10 Layout

10.1 Layout Guidelines

Proper grounding and proper routing of all signals is essential to ensure accurate conversion. Each ground layer should be a single unified ground plane, rather than splitting the ground planes into analog and digital areas.

Because digital switching transients are composed largely of high frequency components, the skin effect dictates that the total ground-plane copper weight has little effect upon the logic-generated noise. Total surface area is more important than the total ground-plane volume. Coupling between the typically-noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that can be impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High-power digital components must not be located on or near any linear component or power-supply trace or plane that services analog or mixed-signal components because the resulting common return current path could cause fluctuation in the analog input *ground* return of the ADC which causes excessive noise in the conversion result.

In general, assume that analog and digital lines must cross each other at 90° to avoid digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. The input clock lines must be isolated from **all** other lines, both analog and digital. The generally-accepted 90° crossing must be avoided because even a same amount of coupling causes problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

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Layout Guidelines (continued)

Coupling onto or between the clock and input signal paths must be avoided using any isolation techniques available including distance isolation, orientation planning to prevent field coupling of components like inductors and transformers, and providing well coupled reference planes. Via stitching around the clock signal path and the input analog signal path provides a quiet ground reference for the critical signal paths and reduces noise coupling onto these paths. Sensitive signal traces must not cross other signal traces or power routing on adjacent PCB layers, rather a ground plane must separate the traces. If necessary, the traces should cross at 90° angles to minimize crosstalk.

Isolation of the analog input is important because of the low-level drive required of the ADC12J1600 and ADC12J2700 devices. Quality analog input signal and clock signal path layout is required for full dynamic performance. Symmetry of the differential signal paths and discrete components in the path is mandatory and symmetrical shunt-oriented components should have a common grounding via. The high frequency requirements of the input and clock signal paths necessitate using differential routing with controlled impedances and minimizing signal path stubs (including vias) when possible.

Layout of the high-speed serial-data lines is of particular importance. These traces must be routed as tightly coupled 100-Ω differential pairs, with minimal vias. When vias must be used, care must be taken to implement control-impedance vias (that is, 50-Ω) with adjacent ground vias for image current control.

10.2 Layout Example

The following examples show layout-example plots (top and bottom layers only). Figure 117 shows a typical stackup for a 10 layer board.

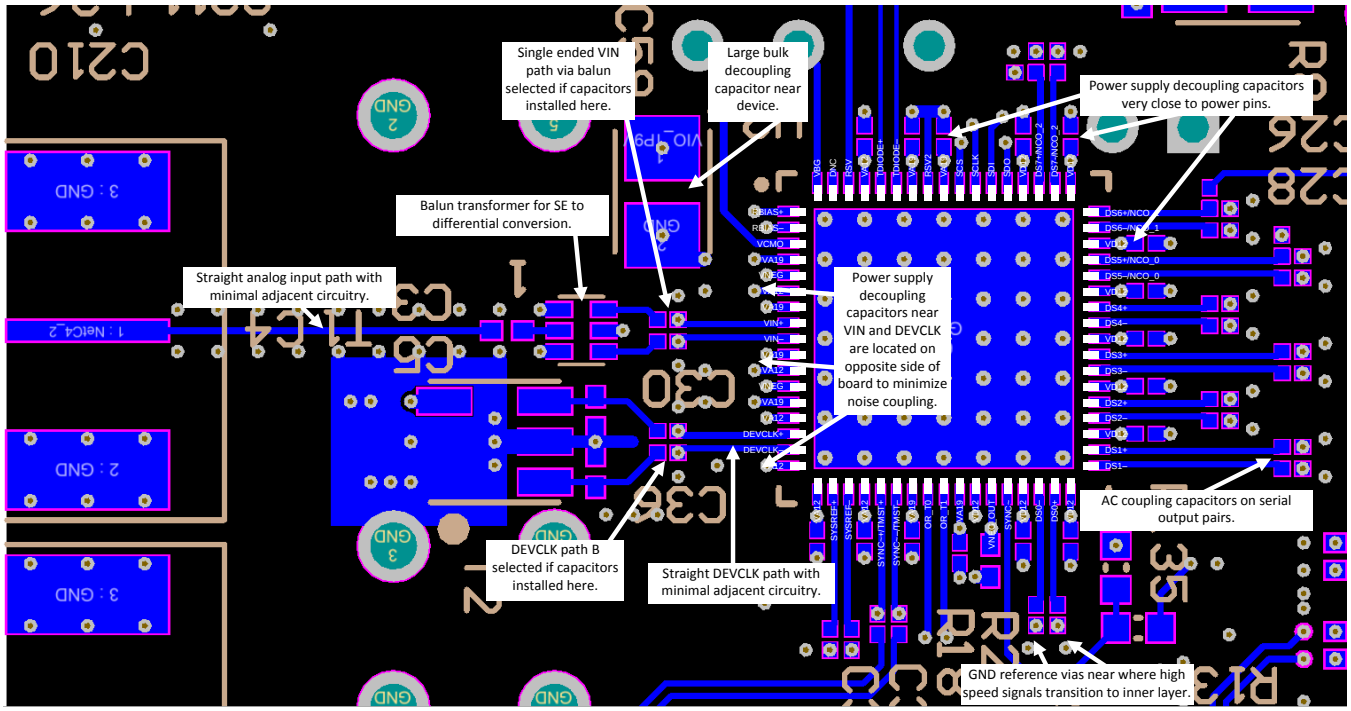

Figure 115. ADC12J1600 and ADC12J2700 Layout Example 1 — Top Side

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Layout Example (continued)

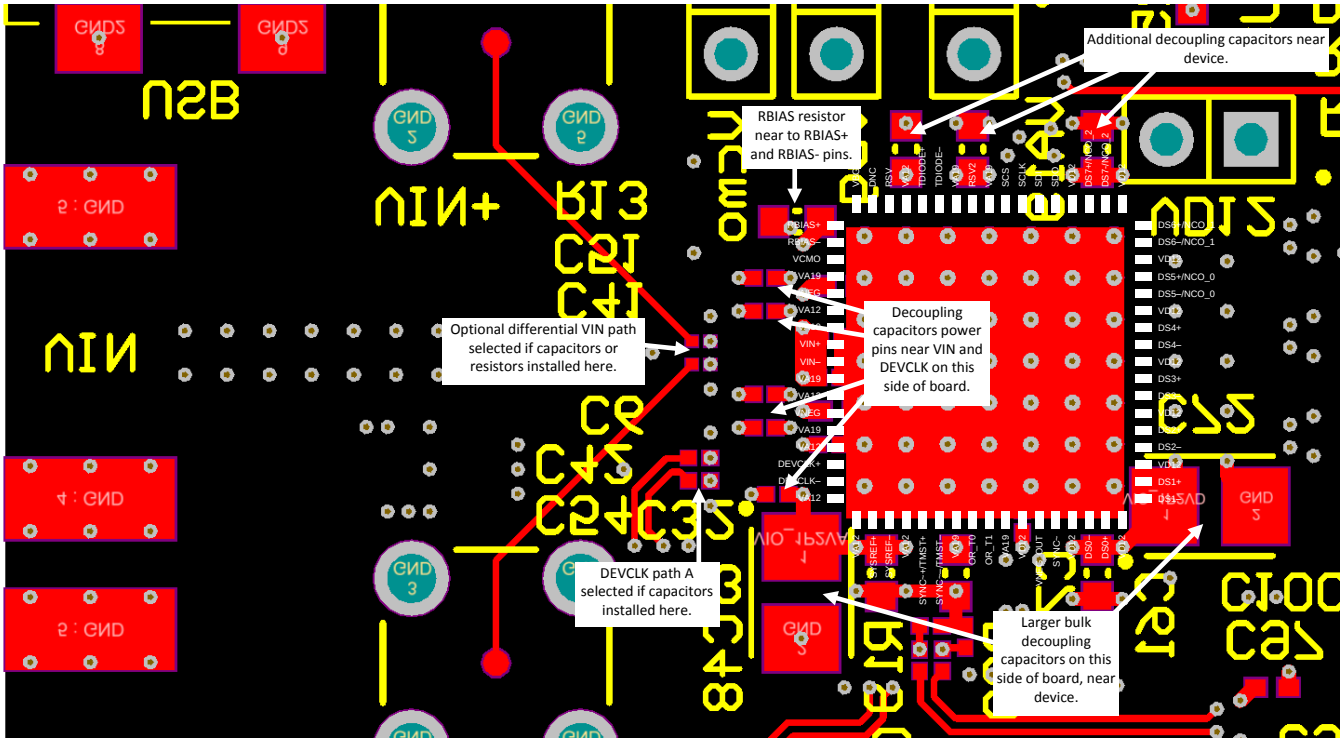
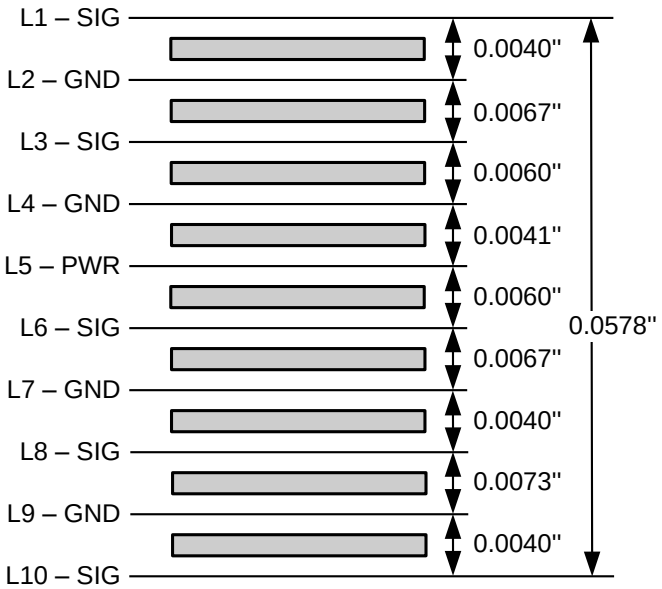


Figure 116. ADC12J1600 and ADC12J2700 Layout Example 2 — Bottom Side



1/2 oz. Copper on L1, L3, L6, L8, L10
1 oz. Copper on L2, L4, L5, L7, L9
100 Differential Signaling on SIG Layers
Low loss dielectric adjacent very high speed trace layers
Finished thickness 0.0620" including plating and solder mask

Figure 117. ADC12J1600 and ADC12J2700 Typical Stackup — 10 Layer Board

10.3 Thermal Management

The ADC12J1600 and ADC12J2700 devices are capable of impressive speeds and performance at low power levels for speed. However, the power consumption is still high enough to require attention to thermal management. The VQFN package has a primary-heat transfer path through the center pad on the bottom of the package. The thermal resistance of this path is provided as $R_{\theta JCbot}$.

For reliability reasons, the die temperature must be kept to a maximum of 135°C which is the ambient temperature (T_A) plus the ADC power consumption multiplied by the net junction-to-ambient thermal resistance ($R_{\theta JA}$). Maintaining this temperature is not a problem if the ambient temperature is kept to a maximum of 85°C as specified in the *Recommended Operating Conditions* table and the center ground pad on the bottom of the package is thermally connected to a large-enough copper area of the PC board.

The package of the ADC12J1600 and ADC12J2700 devices have a center pad that provides the primary heat-removal path as well as excellent electrical grounding to the PCB. Recommended land pattern and solder paste examples are provided in the *Mechanical, Packaging, and Orderable Information* section. The center-pad vias shown must be connected to internal ground planes to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

If needed to further reduce junction temperature, TI recommends to build a simple heat sink into the PCB which occurs by including a copper area of about 1 to 2 cm^2 on the opposite side of the PCB. This copper area can be plated or solder-coated to prevent corrosion, but should not have a conformal coating which would provide thermal insulation. Thermal vias will be used to connect these top and bottom copper areas and internal ground planes. These thermal vias act as *heat pipes* to carry the thermal energy from the device side of the board to the opposite side of the board where the heat can be more effectively dissipated.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For the ADC Harmonic Calculator, got to http://www.ti.com/tool/adc-harmonic-calc.

11.1.3 Device Nomenclature

Aperture (sampling) Delay is the amount of delay, measured from the sampling edge of the clock input, after which the signal present at the input pin is sampled inside the device.

Aperture Jitter ($t_{(AJ)}$) is the variation in aperture delay from sample to sample. Aperture jitter appears as input noise.

Clock Duty Cycle is the ratio of the time that the clock waveform is at a logic high to the total time of one clock period.

Full Power Bandwidth (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below the low frequency value for a full scale input.

Interleaving Spurs are frequency domain (FFT) artifacts resulting from non-idealities in the multi-bank interleaved architecture of the ADC.
Offset errors between banks result in fixed spurs at f_S / 4 and f_S / 2. Gain and timing errors result in input-signal-dependent spurs at f_S / 4 ± F_{IN} and f_S / 2 ± F_{IN}.

Intermodulation Distortion (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. IMD is defined as the ratio of the power in the second-order and third-order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

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Device Support (continued)

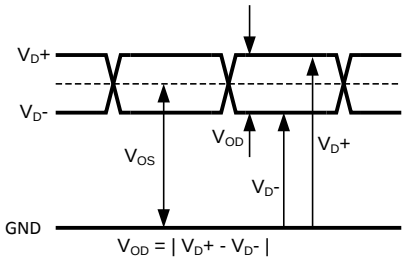
Least Significant Bit (LSB) is the bit that has the smallest value or weight of all bits. This value is calculated with Equation 18.

$$V_{FS(dif)} / 2^n \quad (18)$$

where

- $V_{FS(dif)}$ is the differential full-scale amplitude of V_I as set by the FSR input (pin 14)
- *n* is the ADC resolution in bits, which is 12 for the ADC12J1600 and ADC12J2700 devices

CML Differential Output Voltage (V_{OD}) is the absolute value of the difference between the positive and negative outputs. Each output is measured with respect to Ground.



CML Output Signal Levels

CML Output Offset Voltage ($V_{O(ofs)}$) is the midpoint between the D+ and D– pins output voltage. Equation 19 is an example of V_{OS}.

$$[(V_D+) + (V_D–)] / 2 \quad (19)$$

Most Significant Bit (MSB) is the bit that has the largest value or weight. The value of the MSB is one half of full scale.

Overrange Recovery Time is the time required after the differential input voltages goes from ±1.2 V to 0 V for the converter to recover and make a conversion with its rated accuracy.

Other Spurs is the sum of all higher harmonics (fourth and above), interleaving spurs, and any other fixed or input-dependent spurs.

Data Delay (Latency) is the number of input clock cycles between initiation of conversion and when related data is present at the serializer output.

Spurious-free Dynamic Range (SFDR) is the difference, expressed in dB, between the RMS values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding DC.

Total Harmonic Distortion (THD) is the ratio expressed in dB, of the RMS total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated with Equation 20.

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}} \quad (20)$$

where

- $A_{(f1)}$ is the RMS power of the fundamental (output) frequency
- $A_{(f2)}$ through $A_{(f10)}$ are the RMS power of the first nine harmonic frequencies in the output spectrum

Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency detected at the output and the power in the second harmonic level at the output.

Third Harmonic Distortion (3rd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in the third harmonic level at the output.

Word Error Rate is the probability of error and is defined as the probable number of errors per unit of time divided by the number of words seen in that amount of time. A Word Error Rate of 10^{-18} corresponds to a statistical error in one conversion about every four years.

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *LMH3401 7-GHz, Ultra-Wideband, Fixed-Gain, Fully-Differential Amplifier*, SBOS695
- *LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs*, SNAS605
- *LMX2581 Wideband Frequency Synthesizer with Integrated VCO*, SNAS601
- *TRF3765 Integer-N/Fractional-N PLL with Integrated VCO*, SLWS230

11.3 Related Links

Below are direct links to information available to accelerate design activity. Categories include technical information, community resources, design information, and quick access to sample or purchase once you have made a decision.

Parts	Product Folder	Sample & Buy	Technical Documents	Tools & Software	Support & Community
ADC12J1600	Click here	Click here	Click here	Click here	Click here
ADC12J2700	Click here	Click here	Click here	Click here	Click here

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC12J1600NKE	ACTIVE	VQFN	NKE	68	168	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC12J1600	Samples
ADC12J1600NKER	ACTIVE	VQFN	NKE	68	2000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC12J1600	Samples
ADC12J1600NKET	ACTIVE	VQFN	NKE	68	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC12J1600	Samples
ADC12J2700NKE	ACTIVE	VQFN	NKE	68	168	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC12J2700	Samples
ADC12J2700NKER	ACTIVE	VQFN	NKE	68	2000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC12J2700	Samples
ADC12J2700NKET	ACTIVE	VQFN	NKE	68	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	ADC12J2700	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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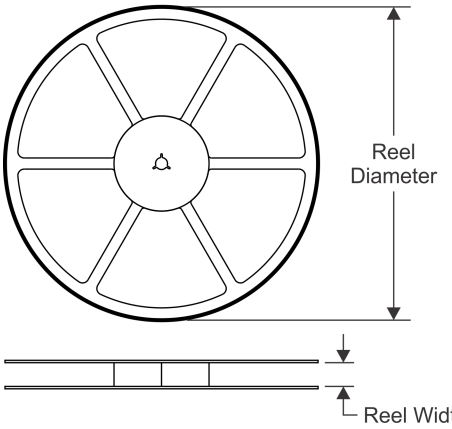
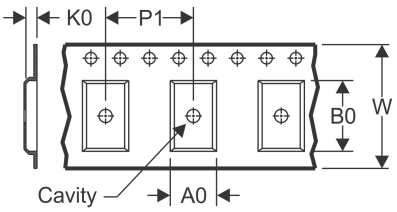
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

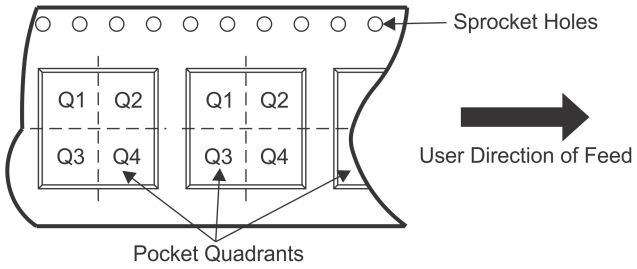


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

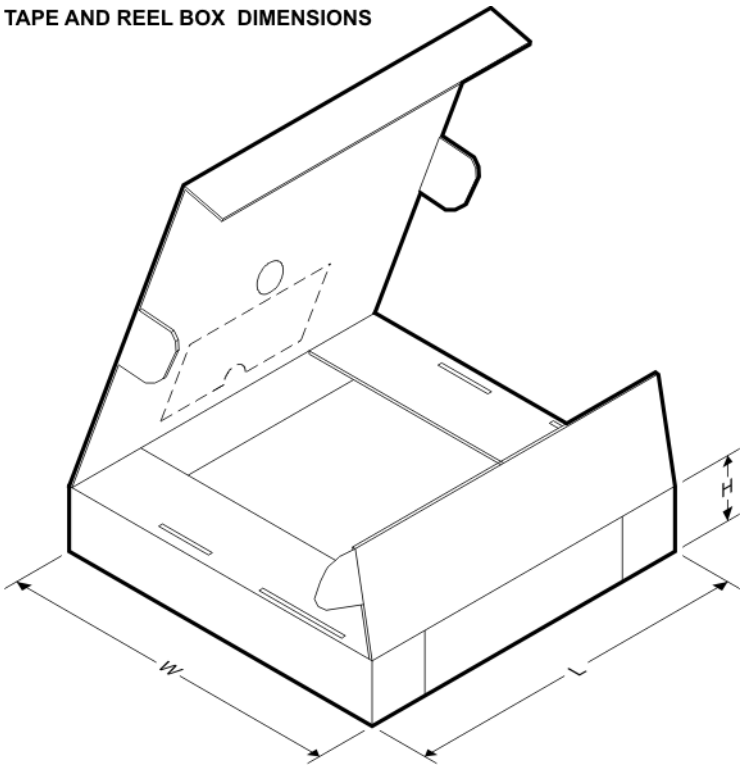
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC12J1600NKET	VQFN	NKE	68	250	178.0	24.4	10.3	10.3	1.1	16.0	24.0	Q1
ADC12J2700NKER	VQFN	NKE	68	2000	330.0	24.4	10.3	10.3	1.1	16.0	24.0	Q1
ADC12J2700NKET	VQFN	NKE	68	250	178.0	24.4	10.3	10.3	1.1	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

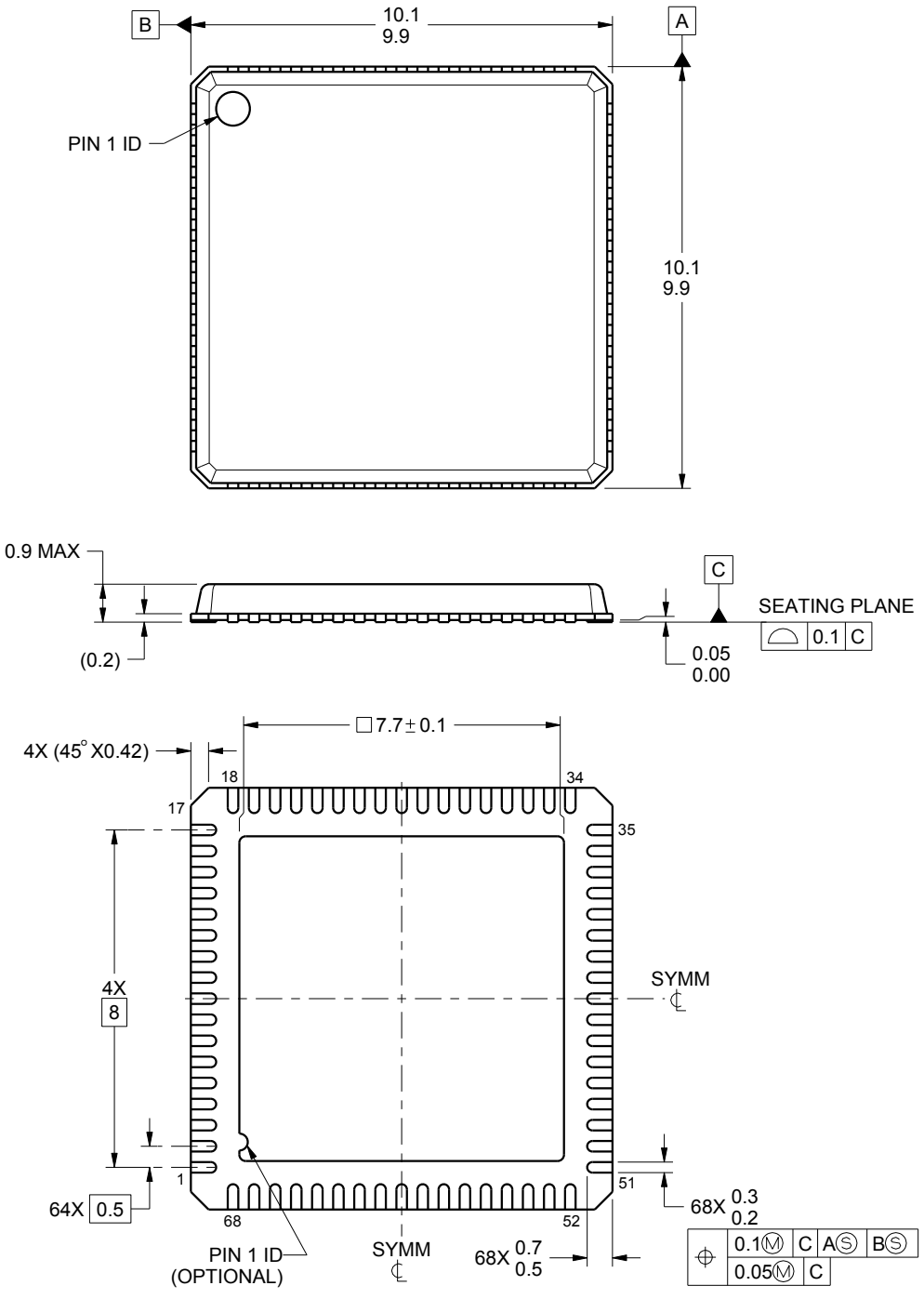
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC12J1600NKET	VQFN	NKE	68	250	213.0	191.0	55.0
ADC12J2700NKER	VQFN	NKE	68	2000	367.0	367.0	45.0
ADC12J2700NKET	VQFN	NKE	68	250	213.0	191.0	55.0

PACKAGE OUTLINE

NKE0068A

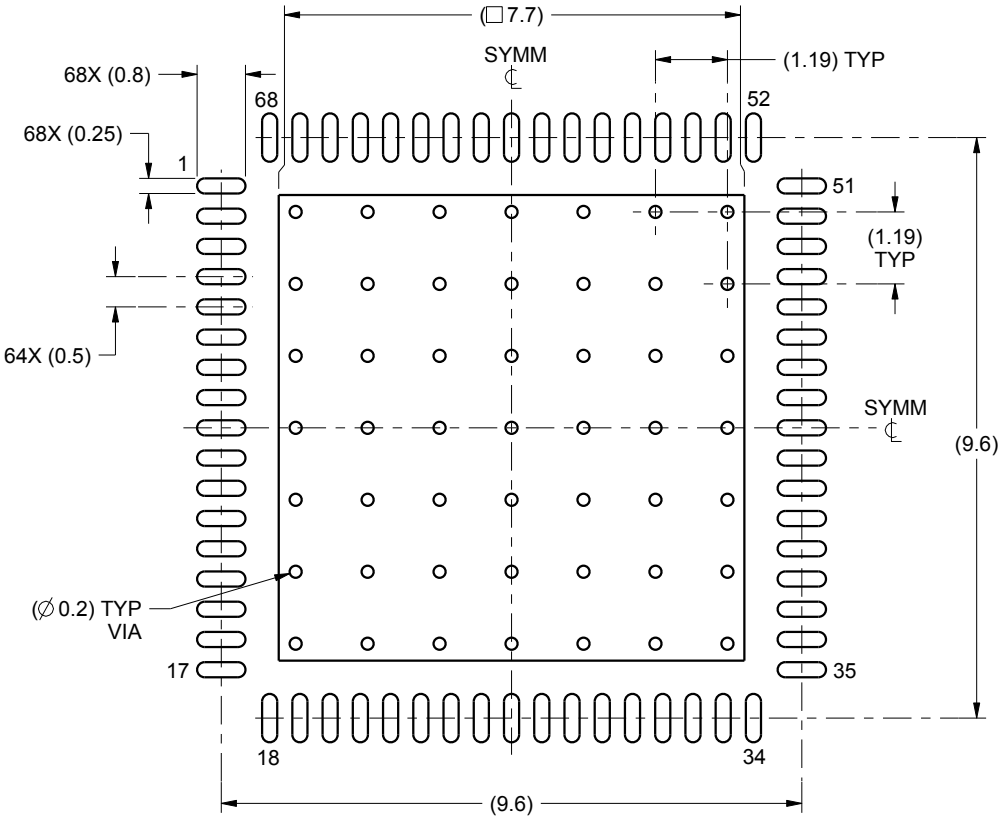
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

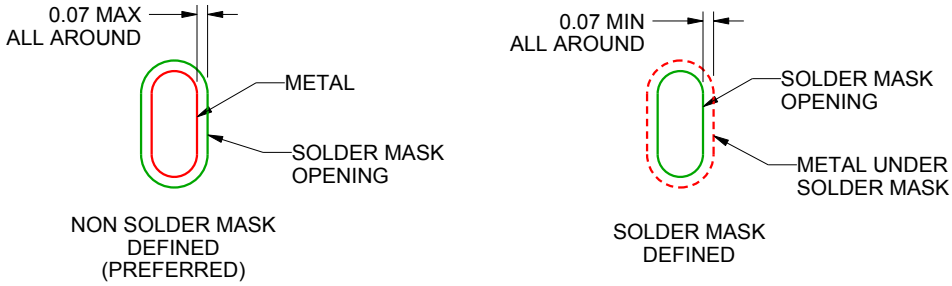


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X

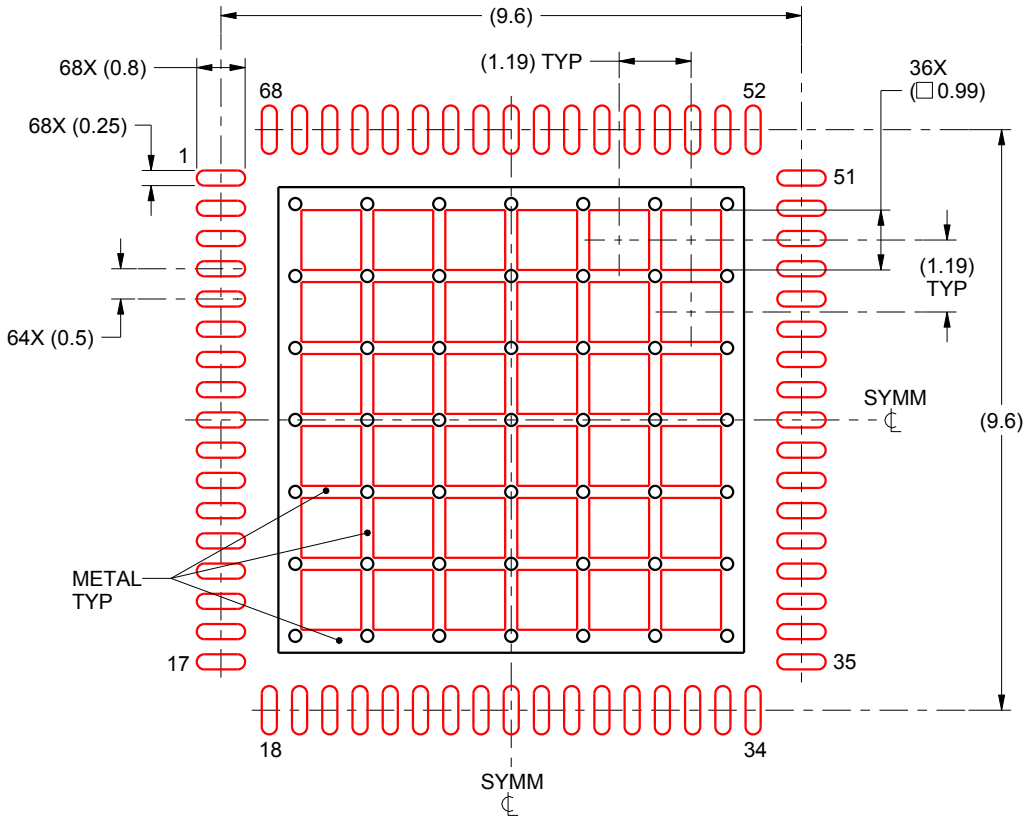


SOLDER MASK DETAILS

4214820/A 12/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4214820/A 12/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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